Supplementary Figures and Tables for

"FeFET CMOS 0.18 μm Integration Study"

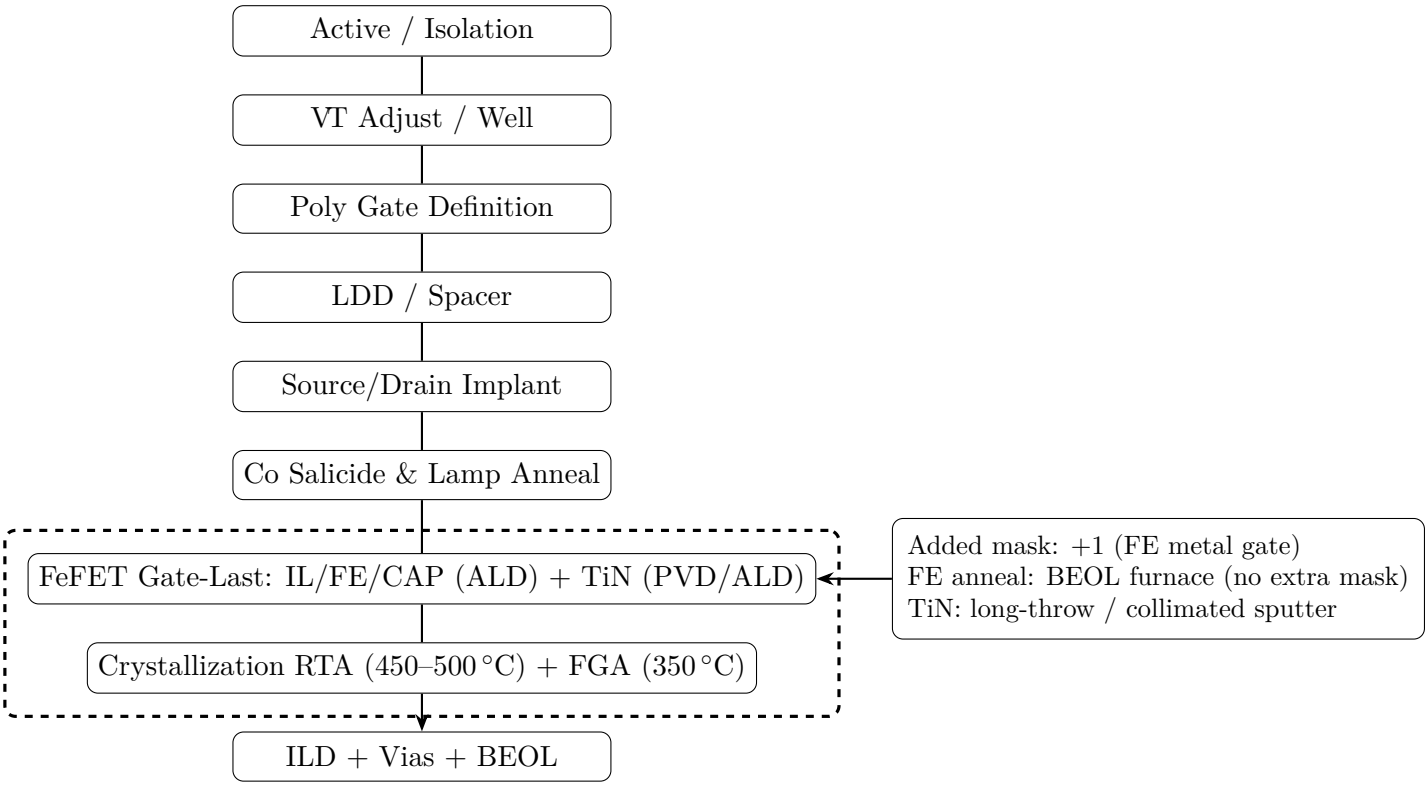


Figure 1: Placement of the FeFET gate-last module within the 0.18 μm CMOS baseline (vertical layout).

Table 1: Added masks / process steps relative to baseline logic.

Step	Mask	Comment
FE metal gate	+1	Reuse analog option route
FE anneal	0	Performed in BEOL furnace (no extra mask)

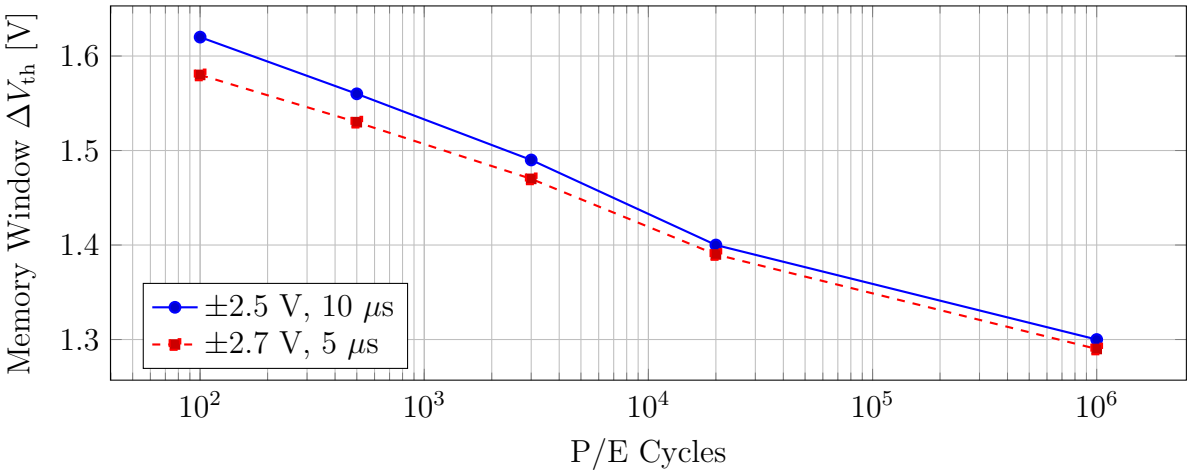
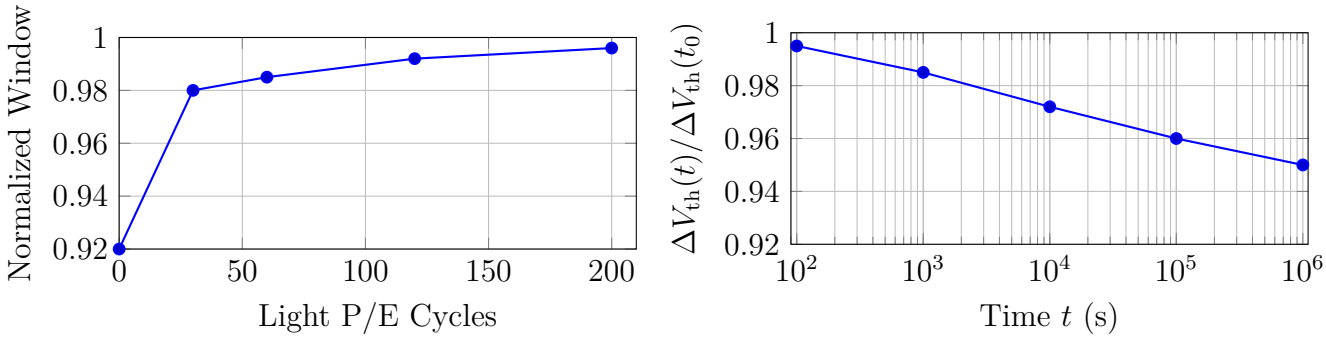


Figure 2: Schematic endurance behavior of HZO-FeFETs in a 0.18 μm flow.



(a) Wake-up **(b)** Retention at 85°C

Figure 3: Wake-up Retention

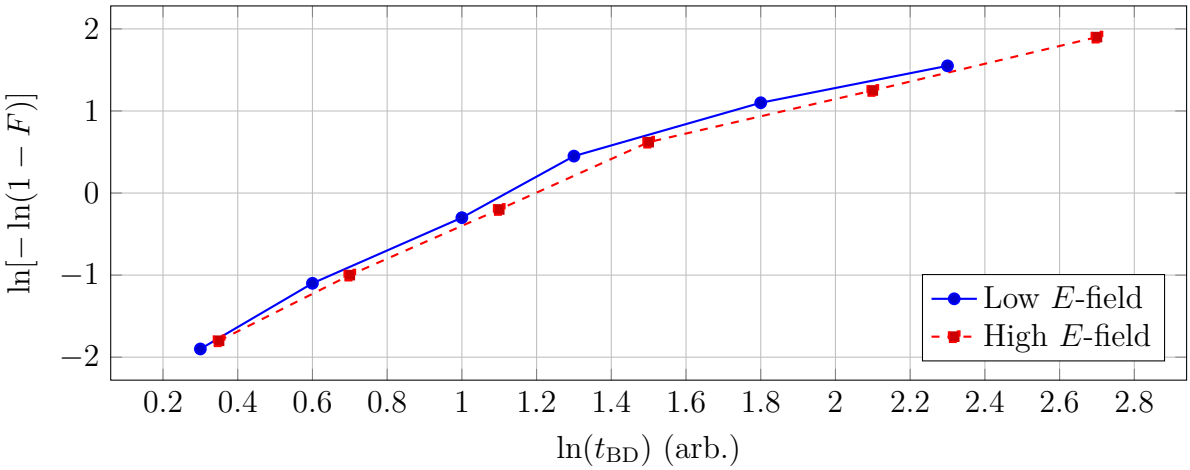


Figure 4: TDDB Weibull representation at two stress fields (illustrative).