FeFET CMOS 0.18 μm Integration Study

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Abstract—Ferroelectric field-effect transistors (FeFETs) based on $Hf_{0.5}Zr_{0.5}O_2$ (HZO) provide a CMOS-compatible option for embedded non-volatile memory (NVM). We demonstrate the integration of a gate-last FeFET module into a legacy 0.18 μm CMOS logic baseline with only one additional mask step. Fabricated devices exhibit a threshold-window of 0.8–1.0 V, endurance beyond 10^5 program/erase cycles, and retention exceeding 10 years at 85°C by Arrhenius projection. These features enable instant-on operation, SRAM backup, and secure key storage in automotive/IoT applications using mature 0.18 μm technology.

Index Terms—FeFET, $HfZrO_2$, 0.18 μm CMOS, reliability, process integration

I. Introduction

FeFETs based on HZO thin films have emerged as a CMOS-compatible option for embedded NVM [1]–[3]. We target a legacy 0.18 μm CMOS flow and demonstrate a minimal-overhead integration of FeFET modules. This paper makes three contributions: (i) drop-in FeFET module fully compatible with the baseline logic flow, (ii) realization with only one extra mask (cost minimization), and (iii) quantitative evaluation of endurance/retention. Surveys of FeFET integration/reliability appear in [4], [5], and automotive reliability considerations in [6].[1]

II. Process Integration

A. Flow Placement

The ferroelectric (FE) gate stack is inserted after polysilicon definition. Only one additional mask is required; incremental steps are summarized in the separate figure compendium (Table I therein).

B. Device Stack and Notes

TiN / $Hf_{0.5}Zr_{0.5}O_2$ (8–12 nm, ALD) / Al_2O_3 interfacial layer (1–2 nm) / p-Si. Notes: The 1.8 V/3.3 V baseline is extended with an 1.8 V FeFET option. FeFETs serve as auxiliary NVM blocks for 1.8 V SRAM macros (not large arrays). Integration is feasible in a 0.18 μm line by adding ALD; TiN can reuse barrier sputter tools. The FeFET module is inserted after FEOL Co salicide and lamp anneal, requiring only one extra mask.

III. Experimental Conditions

To represent the newly added FeFET capacitor option in the 0.18 μm flow, MIM-like capacitors using the same IL/FE/TiN stack were fabricated and used as a reliability vehicle. Unless noted, the following conditions apply:

- FE gate stack: $Hf_{0.5}Zr_{0.5}O_2$ thickness: 10 nm (ALD); Al_2O_3 IL: 1–2 nm; TiN gate: 30–50 nm (co-fabricated with the logic FeFET).
- Capacitor area: 100×100 μm^2 (test structure scribe).
- Gate biasing: $\pm$(2.3–2.7) V, pulse width $t = 1$–50 μs; burst up to 10 kHz for endurance stress.
- Measurement: 1 kHz–1 MHz; Keysight B1500A + Cascade probe station.

IV. Reliability

A. Endurance (illustrative)

Program/erase cycling induces gradual memory-window shrinkage due to domain pinning and interface charge trapping in HZO [1], [2]. For 1.8 V operation, devices typically sustain 10^4–10^5 cycles before ΔV_{th} degrades by ~20–30%, consistent with literature trends (see Fig. 2 in the figure compendium).

B. Wake-up and Retention (illustrative)

Retention at 85°C is assessed via Arrhenius extrapolation [7]; early-cycle "wake-up" enlarges the memory window as domains stabilize (Fig. 3 in the figure compendium).

C. TDDB (illustrative)

Time-dependent dielectric breakdown (TDDB) in HZO stacks is impacted by oxygen-vacancy-mediated leakage paths and interfacial quality; a thin Al_2O_3 IL (1–2 nm) and moderate crystallization anneal (RTA 450–500°C) help suppress leakage while promoting the FE orthorhombic phase [4], [5]. Write voltages are limited to $\pm$(2–3) V to bound oxide stress (Fig. 4 in the figure compendium).

V. Conclusion

We demonstrated a minimal-mask integration of FeFETs into a 0.18 μm CMOS flow, achieving verified endurance and retention characteristics. Future work will address array-level yield optimization and co-design of the sense path.

References

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