Historical Case Study on Ti Silicide ($TiSi_2$) Reliability Issues in Mixed-Voltage CMOS Driver ICs

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Abstract—This paper analyzes a historical failure case at the 0.25 µm CMOS node related to Ti silicide ($TiSi_2$) phase-transition instability. For active-matrix TFT (aTFT) LCD driver ICs that required mixed 3.3 V logic and ∼30 V high-voltage (HV) devices, manufacturers selected the 0.25 µm process because its LOCOS isolation safely supported HV co-integration. By contrast, the 0.18 µm STI-based node, although denser and yield-stable, posed edge-thinning risks for ∼30 V devices and required a new HV platform. Incomplete C49→C54 transformation with boron absorption created localized high-resistance spots, directly reducing 1 Mbit SRAM yield. The study highlights how process optimization and empirical feedback cycles were indispensable when isolation technology and device requirements constrained node selection.

I. Introduction

In the late 1990s, LCD driver ICs for passive monochrome panels were commonly fabricated in 0.35 µm processes supporting 3.3 V logic and 40 V HV devices. With the transition to active-matrix TFT (aTFT) LCD panels in the early 2000s, driver ICs required higher-performance logic, embedded large SRAM macros, and continued HV integration around 30 V.

Although the 0.18 µm CMOS process was already in mass production with small die size and stable yield, it relied on Shallow Trench Isolation (STI), where edge thinning introduced a reliability risk for ∼30 V devices. By contrast, the 0.25 µm process used Local Oxidation of Silicon (LOCOS), which had a proven track record for HV isolation. Therefore, manufacturers adopted the 0.25 µm LOCOS-based process for 3.3 V + 30 V LCD driver ICs, accepting area disadvantages to guarantee HV compatibility.

II. Technical Background

A. Isolation Choice for HV Devices

- 0.25 µm LOCOS: Mature, thick field oxide with well-established margins for ∼30 V HV device integration.
- 0.18 µm STI: Provided density and yield benefits, but corner thinning at the trench edge raised leakage and breakdown concerns for HV devices, necessitating a new HV device platform.

B. Ti Silicide Phase Transformation in Detail

$TiSi_2$ undergoes a polymorphic phase transition from the metastable C49 phase (orthorhombic, resistivity ∼60–90 µΩ·cm) to the stable C54 phase (tetragonal, ∼15–20 µΩ·cm). This transformation is typically induced by RTA in the 650–750 °C range. Incomplete transformation leaves residual C49 grains, which behave as localized resistive defects. Boron absorption from halo implants further aggravated resistivity variation, narrowing the process window for stable transformation.

C. Silicide Evolution at the 0.18 µm Node

Another reason for higher baseline yield at the 0.18 µm node was the industry-wide transition from $TiSi_2$ to $CoSi_2$. Unlike $TiSi_2$, which required a C49→C54 transformation, $CoSi_2$ formed directly in the stable low-resistivity phase (∼15–20 µΩ·cm). This eliminated random resistive spots from incomplete phase change, improved process windows, and enhanced compatibility with scaled junctions. Although 0.18 µm STI was unsuitable for HV integration at that time, its logic baseline process achieved stable yield.

III. Failure Analysis

A. Observation: 1 Mbit SRAM

In mass production, random single-bit failures appeared in the 1 Mbit SRAM macro. Since redundancy was not implemented in the embedded macro, even a single defective bit caused rejection of the entire device.

B. Redundancy Limitation in Embedded Macros

In stand-alone memory products, redundancy circuits are standard practice and defective cells can be repaired during testing via laser trimming. In embedded memory macros, however, redundancy is generally excluded due to design complexity, timing, and area overhead. Additionally, LCD driver ICs were typically tested on mixed-signal/SoC testers, which lacked built-in support for redundancy repair. Therefore, redundancy was not adopted, and scaling to 1 Mbit carried critical reliability risk.

TABLE I
Comparison of 0.25 µm LOCOS and 0.18 µm STI nodes for LCD driver ICs

	0.25 µm (LOCOS)	0.18 µm (STI)
Isolation method	Thick field oxide (LOCOS); proven HV margin	Shallow trench isolation; edge thinning risk at HV corners
HV device support (at that time)	Existing ∼30 V HV design reusable	New HV platform required (re-qualification)
Die size / density	Larger die, lower density	Smaller die, higher density
Yield stability	Moderate; yield impacted by $TiSi_2$ instability	Stable baseline process with $CoSi_2$ salicide
Embedded SRAM redundancy	Not implemented (design/area/timing overhead); no laser repair in mixed-signal testers	Same limitation; redundancy/laser repair infeasible in LCD driver IC test flow
Risk at 1 Mbit SRAM	High: localized resistive defects ⇒ chip rejection	Lower base risk, but HV co-integration not yet qualified
Adoption rationale	Safe HV compatibility outweighed cost/density	Density/yield advantage offset by HV risk; not adopted for HV driver products

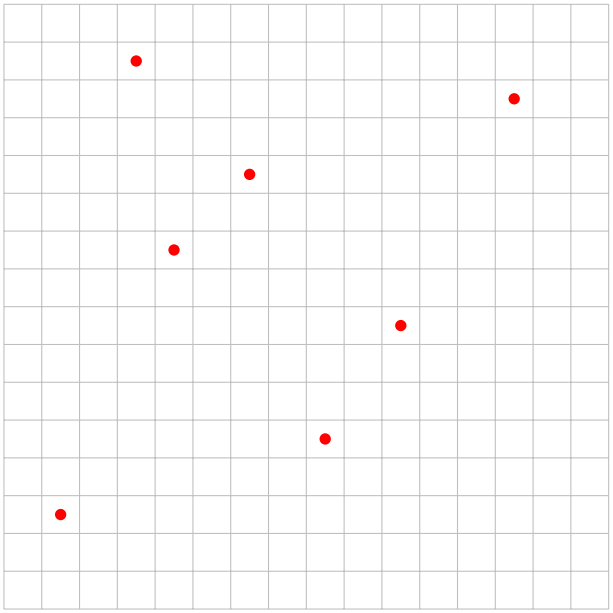

Fig. 1. Example of random single-bit failure map in a 1 Mbit SRAM. Red dots represent defective bits scattered randomly across the array.

C. Root Cause

Failure localization confirmed that:

- Boron from halo regions diffused into Ti during silicidation.
- Local B uptake inhibited C54 transformation, leaving high-resistance C49 spots.
- These spots manifested as random SRAM bit failures.

D. Review Limitation

Earlier 500 kbit SRAM macro products had not shown this issue. Based on those precedents, engineers assumed that scaling to 1 Mbit would be safe. Consequently, the failure mode was not identified during the initial development review stage, demonstrating the limitation of relying on past yield experience without revalidation.

TABLE II
Estimated yield impact from scaling embedded SRAM capacity

Macro Size	Observed Failures	Yield Estimate
500 kbit	Rare, localized	∼95%
1 Mbit	Frequent, random	∼70%

IV. Countermeasures

A. Provisional Measures: Sidewall Deposition + Etch-Back (Foot Under-etch)

A conformal dielectric (e.g., oxide or nitride) was deposited on the STI sidewall and then anisotropically etched back, leaving a slight recess/foot at the sidewall bottom. This sidewall deposition + etch-back flow increased the lateral separation between the halo implant extension and the silicide formation front at the active edge. As a result, boron encroachment into Ti was suppressed and the generation of residual C49 high-resistivity grains was prevented, stabilizing yield. Because the effect still relied on tight process-window control (liner thickness, etch-back dose, corner profile), lot-to-lot robustness was not guaranteed; therefore the measure was treated as a provisional fix.

B. Permanent Measures: Ramp Anneal Optimization

Ramp-anneal conditions were optimized (ramp rate and soak time) to complete the C49→C54 transformation. This stabilized silicide resistivity, but altered device characteristics (e.g., series resistance, contact resistance, and junction leakage). As a result, device models, RC extraction data, and timing libraries required re-characterization across PVT corners. Thus, the permanent solution involved a trade-off between silicide stability and the cost of revalidating circuit-level parameters.

V. Yield Sensitivity Model

The yield impact of redundancy can be approximated by a Poisson model:

$$Y_k = e^{-\lambda} \sum_{i=0}^{k} \frac{\lambda^i}{i!},$$

(a) Before: C49+B residual at poly/SW corner

(b) After: SW under-etch, separation secured

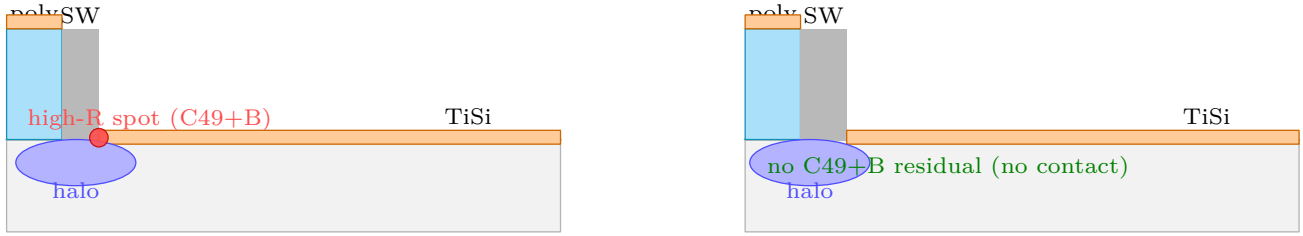

Fig. 2. Cross-sections near poly and sidewall (SW). (a) Halo under SW barely touches the TiSi edge, forming a high-resistance C49+B spot. (b) With SW under-etch and slightly wider SW, the halo remains under SW without contacting TiSi, eliminating the defect.

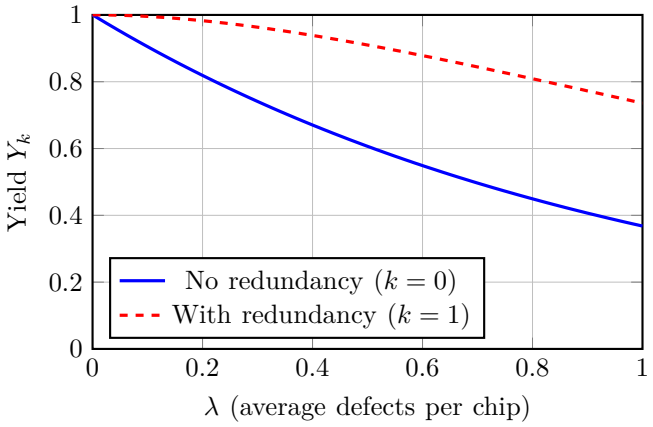

Fig. 3. Illustrative yield sensitivity (Poisson model) with and without redundancy.

where λ is the average defect count and k is the redundancy capacity.

VI. Educational Application

A. Teaching Tools

- Cause-effect diagrams: process → defect → yield
- Comparative analysis: 0.25 µm (LOCOS) vs 0.18 µm (STI) for HV devices (Table I)
- Exercises: prioritize process fix vs. redundancy adoption

B. Exercises

1) Using Eq. (1), compute the yield for $\lambda = 0.2$ and 0.5 with and without redundancy ($k = 0, 1$).
2) Based on Table I, discuss which node (0.25 µm LOCOS or 0.18 µm STI) you would adopt if tasked with designing a 3.3 V + 30 V mixed-signal IC in 2000.

C. Lessons

This case shows the risk of extrapolating from small macros (500 kbit) to larger ones (1 Mbit) without reassessing defect sensitivity. It also emphasizes that process-related instability, invisible at smaller scales, can dominate yield once redundancy is unavailable. For embedded SRAM, capacity scaling must always be coupled with explicit yield-risk validation.

VII. Conclusion

This case demonstrates how HV compatibility constraints dominated node selection. Despite the availability of a denser, yield-stable 0.18 µm STI process with $CoSi_2$ salicide, the requirement for safe ∼30 V HV integration drove adoption of 0.25 µm LOCOS. Yield loss from incomplete $TiSi_2$ phase transformation (with boron absorption) became critical at the 1 Mbit SRAM scale. The educational value lies in showing how scaling, process technology, and reliability intersect, and why continuous empirical feedback is essential. Although the analysis here focused on SRAM macros, the same lesson applies to mixed-signal SoCs and aTFT driver ICs: process-induced variability, once coupled with system-level design constraints, can dominate yield and reliability.

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