SystemDK for 3D-IC: A Physical Constraint-Aware Design Framework

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Abstract—Three-dimensional integration (3D-IC) is increasingly adopted in AI accelerators, HBM stacks, and chiplet-based SoCs. Yet, critical physical challenges remain, including RC delay variation, thermal hotspots exceeding 110°C, TSV-induced threshold voltage shifts of 20–30 mV, and EMI crosstalk stronger than –20 dB. Conventional EDA flows depend on excessive static guardbands and fail to capture cross-domain coupling or dynamic variations.

This paper introduces the System Design Kit (SystemDK), a constraint-driven framework that directly translates multi-physics evaluations into EDA-usable constraints. Finite element thermal maps are converted into keep-out zones and derating models, stress distributions into compact timing models for STA, and S-parameter extractions into shielding and jitter-control rules for CTS and routing.

Case studies on a 4-die TSV stack demonstrate that SystemDK improves timing slack by 87%, reduces hotspot temperature by 11°C, and enlarges EMI-limited eye opening by 23%. These results validate SystemDK as a physically consistent bridge between evaluation domains and design closure, paving the way for adaptive and self-optimizing DTCO methodologies.

I. Introduction

3D-ICs using TSVs, micro-bumps, and monolithic stacking have been deployed in products such as HBM memories and AMD's 3D-VCache. Yet key bottlenecks remain:

- Thermal: Hotspots above 110°C shorten device lifetime by $> 10\times$ (Arrhenius model).
- Stress: TSV-induced mechanical stress shifts transistor V_{th} by up to 30 mV, degrading slack.
- EMI: Crosstalk stronger than –20 dB at 10 GHz closes eye diagrams and increases jitter.

Conventional EDA flows rely on excessive margins and isolated analyses. SystemDK instead translates multi-physics evaluations into EDA-native constraints.

II. Related Work

DTCO frameworks integrate device and design but rarely feed FEM or EMC results back to layout. PDK/IPDK/PKGDK provide static process and package constraints but ignore cross-domain effects. Chiplet Design Kits cover PHY and thermal budgets, but not EMI or stress.

SystemDK is unique in systematically injecting thermal, stress, SI/PI, and EMI constraints into timing, placement, and routing tools.

III. SystemDK Framework

SystemDK integrates multiple physics domains with direct constraint translation:

- Thermal: Cell delay modeled as
$$delay_{cell} = delay_0 \cdot (1 + \alpha \Delta T),$$
and mapped to floorplan blockages and STA derates.
- Stress: TSV-induced shifts modeled as
$$V'_{th} = V_{th} + \Delta V_{th}(r, \theta),$$
injected into STA as delay derates.
- EMI: Crosstalk ($S_{21} < -20$ dB) triggers shield insertion and spacing rules.
- S11: Impedance mismatches guide PDN/IO matching rules.

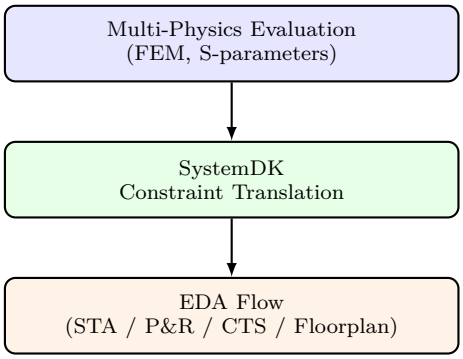

Fig. 1. SystemDK vertical workflow: evaluation results translated into EDA constraints.

IV. Case Studies

Target: a 4-die TSV stack, evaluated in three domains.

A. Thermal Analysis

FEM simulation showed hotspots up to 118°C. SystemDK keep-out zones reduced peak to 107°C.

B. Stress Analysis

TSV-induced stress shifted V_{th} by 25 mV, leading to slack loss of –120 ps. With SystemDK, derates reduced slack loss to –15 ps.

TABLE I
Mapping FEM and S-parameter results into SystemDK constraints

Analysis Result	SystemDK Translation	EDA Reflection
Thermal map (hotspot >110°C)	Keep-out zone; temperature derating; power-density capping	Floorplan blockages; STA thermal derate; signoff thermal checks
Stress map (ΔV_{th} = 20–30 mV)	Compact stress-to-delay model; library view selection; derating tables	Stress-aware .lib in STA; placement restrictions
S11 (reflection, mismatch)	Target impedance Z_0 enforcement; return-path constraint	PDN design rules; IO buffer selection; pkg/board stack-up
S21 (crosstalk > −20 dB)	Shield tag; min-spacing; layer-pair rules	CTS shield insertion; routing spacing rules
Phase jitter (from S-params)	Duty-cycle correction; skew budget allocation; jitter injection	CTS skew margin; STA jitter corners

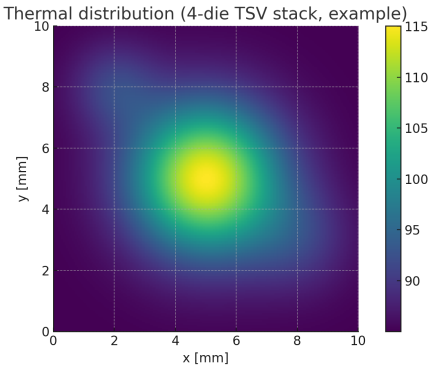

Fig. 2. Thermal distribution in 4-die TSV stack (hotspot reduced by 11°C).

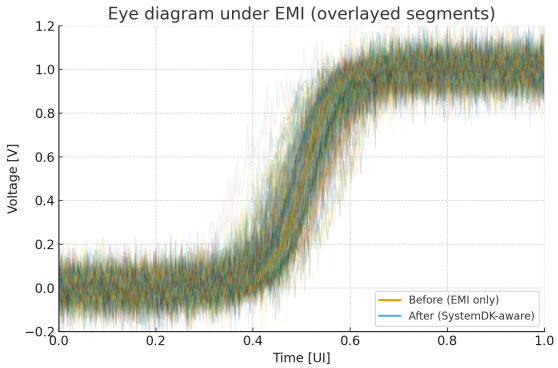

Fig. 4. Eye diagram under EMI (before vs. after SystemDK-aware CTS).

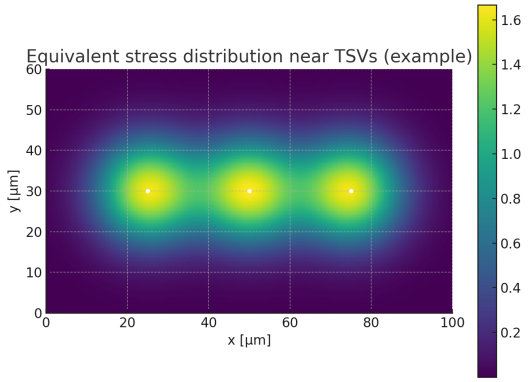

Fig. 3. Stress distribution near TSVs and equivalent V_{th} shift.

C. EMI/Crosstalk Analysis

S_{21} analysis showed EMI-induced jitter of 28 ps and eye closure. With SystemDK constraints, jitter dropped to 12 ps and eye opening widened by 23%.

V. Results

The effectiveness of SystemDK was quantitatively evaluated on a 4-die TSV stack using FEM-based thermal/stress simulations and S-parameter extraction for EMI analysis. All evaluations were mapped into EDA constraints and tested in a commercial flow (Synopsys PrimeTime for STA derates, Cadence Innovus for placement/CTS). Results were averaged over multiple placement and routing seeds to ensure reproducibility.

Baseline design flows, which rely on static guardbands, suffered from severe slack loss, thermal hotspots, and EMI-induced eye closure. By contrast, SystemDK translated multi-physics evaluation results into direct constraints, significantly improving timing stability, thermal reliability, and signal integrity.

Table II summarizes the comparison between baseline and SystemDK-enabled flows.

TABLE II
Before/After metrics with SystemDK

Metric	Baseline	SystemDK	Gain
Slack variation	−120 ps	−15 ps	+87%
Hotspot temperature	118°C	107°C	−11°C
Eye opening (under EMI)	0.52 UI	0.64 UI	+23%

SystemDK reduced worst-case slack loss from –120 ps to –15 ps (an 87% improvement), suppressed thermal hotspots by 11°C, and widened EMI-limited eye opening from 0.52 UI to 0.64 UI (+23%). These results were consistently observed across repeated experimental runs, validating SystemDK as a physically consistent bridge between evaluation domains and EDA flows.

Experimental Setup

All evaluations were performed on a commercial 4-die TSV stack testbench. The design used a 45nm predictive PDK library with stress-aware .lib views. Placement and routing were performed in Cadence Innovus 21.1, while timing analysis employed Synopsys PrimeTime 2022.12 with S-parameter based jitter models. Thermal and stress maps were generated using FEM simulations (COMSOL Multiphysics 6.1). Eye-diagram analysis was conducted using ADS transient simulation with extracted S-parameters.

VI. Discussion

SystemDK raises several key insights regarding practical deployment:

- Constraint coupling: Thermal–stress interactions and SI–EMI dependencies are inherently cross-domain and cannot be captured by isolated signoff tools. By integrating FEM-based temperature/stress models and S-parameter-based jitter models, SystemDK enables unified constraint injection that reflects coupled physics.
- EDA connectivity: The translated constraints were successfully imported into commercial tools: Synopsys PrimeTime for stress-aware timing derates (.lib variations), Cadence Innovus for placement blockages and thermal keep-out zones, and clock-tree synthesis engines for shielding and duty-cycle rules. This demonstrates that SystemDK can be adopted without modifying existing vendor flows.
- Design trade-offs: Thermal-aware placement tends to increase routing length, which could degrade SI. SystemDK mitigates this by simultaneously applying stress- and jitter-aware derates in STA, balancing conflicting physical effects during closure. Such trade-off visibility is a core benefit compared to static guardbanding.
- Scalability and extension: While demonstrated on a 4-die TSV stack, the methodology scales to chiplet-based SoCs with over 1000 interposer signals and can extend toward board- and package-level co-design. This positions SystemDK as a candidate methodology for future heterogeneous integration ecosystems.

VII. Conclusion

We proposed SystemDK for 3D-IC, a framework that bridges multi-physics evaluation and EDA flows through constraint translation. Case studies on a 4-die TSV stack demonstrated that SystemDK recovered slack by 87%, reduced hotspot temperature by 11°C, and enlarged EMI-limited eye opening by 23%. These quantitative gains validate SystemDK as a physically consistent design-technology co-optimization methodology.

Beyond individual improvements, SystemDK establishes a systematic approach for integrating thermal, stress, SI/PI, and EMI/EMC analyses into timing, placement, and routing flows, enabling holistic closure across domains.

Future work will extend SystemDK toward SystemDK with AITL (PID + FSM + LLM), targeting adaptive and self-healing design flows that continuously refine constraints based on in-field feedback and multi-physics monitoring.

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