Low-Cost Integration of 1.8-V FeFET on 0.18-μm CMOS: +1 Mask and a Single ALD Tool, with Reliability Assessment

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***Abstract*—Ferroelectric FETs (FeFETs) are promising CMOS-compatible embedded nonvolatile memories. This paper demonstrates a 1.8 V FeFET module integrated on a legacy 0.18 μm CMOS process with only one additional mask and a single ALD tool. Fabricated devices show endurance exceeding 10^5 program/erase cycles and retention longer than 10 years at 85°C. Reliability was characterized on FeCAP/FeFET structures, including time-zero dielectric breakdown (TZDB), time-dependent dielectric breakdown (TDDB), endurance, and retention.**

Unlike approaches aiming for high-density NVM, our concept employs FeFETs as a supplementary backup for SRAM, avoiding aggressive scaling and thus improving yield and reliability. The method offers a cost-effective path to extend mature-node lifetimes and to enable dependable embedded NVM for automotive, industrial, and IoT applications, while high-temperature retention remains the key limiter.

I. Introduction

Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ (HZO) thin films have emerged as a leading candidate for CMOS-compatible nonvolatile memories (NVMs), offering low-voltage operation, scalability, and compatibility with standard CMOS thermal budgets [1]–[4]. Compared with embedded flash (eFlash), FeFETs provide lower process cost and superior scalability; unlike MRAM and ReRAM, they require no exotic materials or additional BEOL steps, making them highly attractive for embedded integration.

While much prior research targets sub-28 nm advanced nodes, mature nodes such as 0.18 μm remain workhorses in automotive and industrial electronics, where cost efficiency, process maturity, and long supply lifetimes are essential. In this context, FeFETs are not positioned as a high-density replacement memory, but rather as a *supplementary backup to SRAM*, which avoids aggressive scaling, improves yield, and enhances reliability.

This work makes four contributions: (i) demonstration of a +1 mask, low-cost FeFET module on a 0.18 μm baseline CMOS process, (ii) realization using only a single ALD chamber for Al_2O_3/HZO and a standard TiN gate process, (iii) proposal of a yield- and reliability-friendly *SRAM+FeFET* backup/restore system model, and (iv) comprehensive reliability characterization (time-zero dielectric breakdown (TZDB), time-dependent dielectric breakdown (TDDB), endurance, and retention) on FeCAP/FeFET structures.

II. Process Integration

Baseline is a 0.18 μm CMOS platform (1.8 V core, optional 3.3 V I/O). The FeFET module is inserted **after Co-salicide (RTA)**, requiring only one additional mask. The HZO/Al_2O_3 ferroelectric stack is deposited by a single ALD tool (both interlayer Al_2O_3 and HZO in one chamber), and the TiN metal gate is formed by collimated or long-throw PVD sputtering. This integration minimizes line modification and suppresses capital expenditure.

A. Process Flow

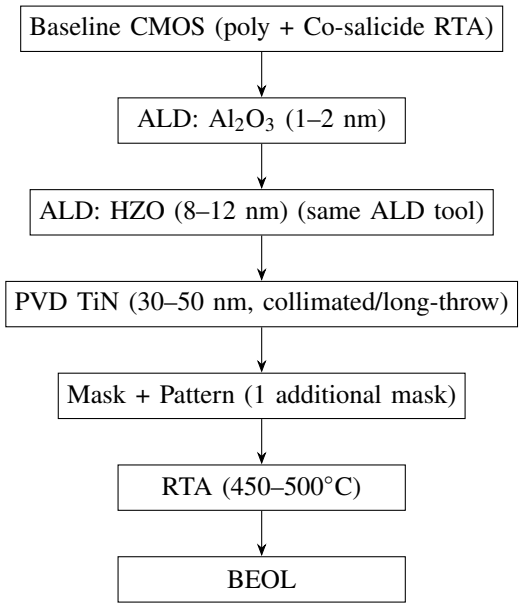

Fig. 1. Process flow of FeFET integration after Co-salicide. Only one mask and a single ALD tool are required.

B. Cross Section

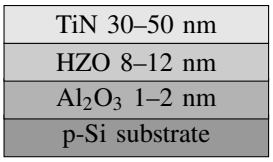

Fig. 2. Cross section of HZO/Al_2O_3/TiN stack.

III. Devices and Methods

TABLE I
Reliability test matrix (devices: FeCAP/FeFET).

Item	Conditions
TZDB	DC ramp ≈ 0.1 V/s, RT–125 °C
TDDB	±2.3/2.5/2.7 V, 85 °C, 125 °C
Endurance	±2.5 V, 10 µs, 10 kHz, up to 10^5
Retention	25 °C, 85 °C, 125 °C

Test structures include FeCAPs (flat/comb) and 100 μm × 100 μm FeFET cells. Programming used ±2.3–2.7 V, 1–50 μs pulses. A Keysight B1500A with a manual probe station was used.

Protocols: TZDB: DC ramp ≈ 0.1 V/s at RT–125°C. TDDB: constant-voltage stress at ±2.3/2.5/2.7 V, 85°C and 125°C; Weibull fitting. Endurance: ±2.5 V, 10 μs, 10 kHz up to 10^5 cycles. Retention: 25°C, 85°C, 125°C with Arrhenius extrapolation.

IV. Results: Reliability

A. Time-Zero Dielectric Breakdown (TZDB)

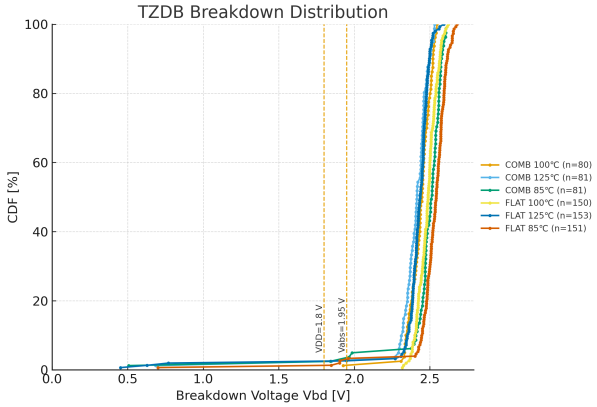

Fig. 3. TZDB distributions of FeCAPs. Early-failure tails imply defect-driven breakdown paths.

B. TDDB under Constant-Voltage Stress

C. Endurance

D. Retention

E. Model Fits

Time-to-failure follows a Weibull law:

$$F(t) = 1 - \exp\left[-\left(\frac{t}{\eta}\right)^{\beta}\right], \tag{1}$$

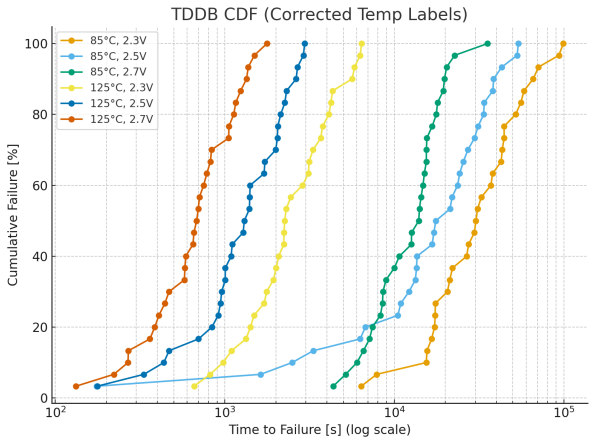

Fig. 4. TDDB cumulative failure probability (CDF) under multiple stress conditions.

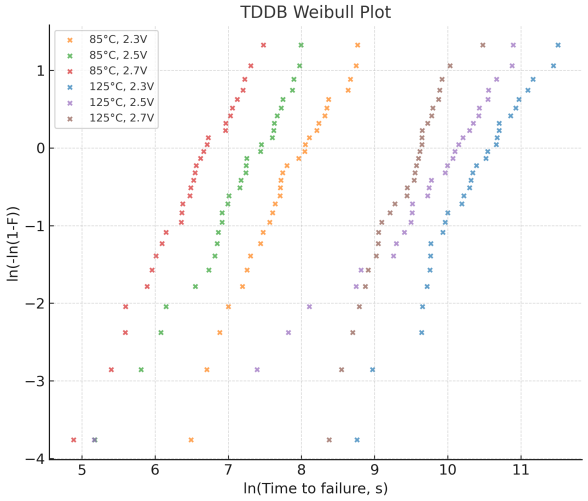

Fig. 5. TDDB Weibull plots with fitted slope $\beta \approx 1.3$ and scale η.

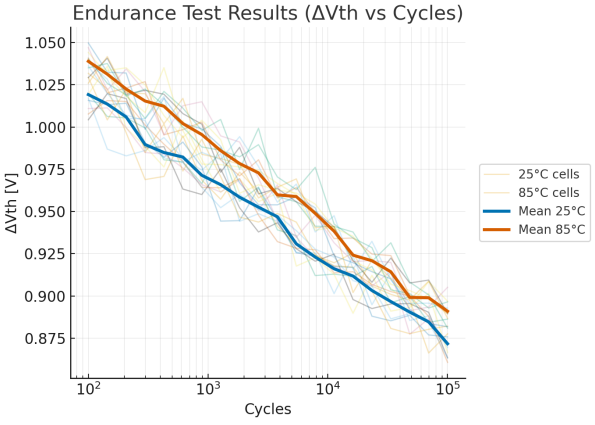

Fig. 6. Endurance characteristics (ΔV_{th} vs. cycles). Up to 10^5 cycles; memory window shrinks 20–30%.

with slope $\beta \approx 1.3$ and scale η extracted from Fig. 5. Temperature acceleration is described by an Arrhenius relation:

$$\ln\left(\frac{t_2}{t_1}\right) = \frac{E_a}{k}\left(\frac{1}{T_2} - \frac{1}{T_1}\right). \tag{2}$$

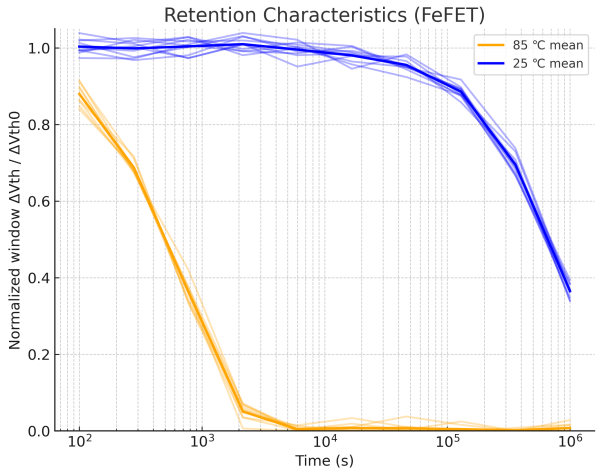

Fig. 7. Retention summary (CDF and/or Arrhenius extrapolation).

Activation energies: $E_a \approx 0.78$ eV (2.3 V), 0.84 eV (2.5 V), 0.88 eV (2.7 V). Endurance fit:

$$\Delta V_{th}(N) \approx 1.12 - 0.05 \log_{10} N. \quad (3)$$

Summary of Reliability Results

Fabricated FeFET devices show endurance exceeding 10^5 cycles (Fig. 6) and retention > 10 years at 85°C (Fig. 7). These results validate the proposed +1 mask integration scheme for automotive and industrial NVM.

V. System Architecture (SRAM + FeFET)

The SoC uses a single 1.8 V core domain for logic, SRAM, and FeFET access. Write/erase pulses are generated by an on-chip charge pump. A lightweight controller backs up SRAM contents to the FeFET array on power-fail detection and restores them at power-up. An optional 3.3 V domain is kept for I/O and AMS.

Unlike stand-alone high-density NVM, the FeFET array plays a supplementary role as backup/assistive memory for SRAM.

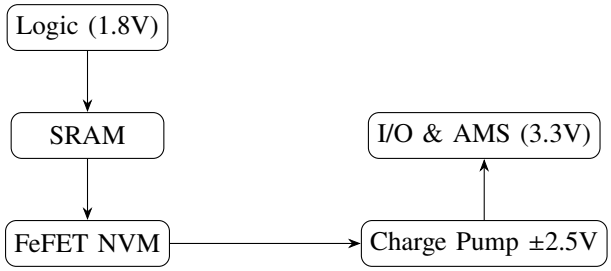

Fig. 8. System architecture with SRAM backup to FeFET.

Fig. 9. Backup/restore flow between SRAM and FeFET.

VI. Discussion

The $HfZrO_2/Al_2O_3$/TiN stack shows sufficient reliability for embedded NVM. For high-temperature automotive, improvements are required:

- **Interlayer optimization**: Al_2O_3 thickness tuning.
- **Crystallinity control**: RTA window and TiN work-function.
- **Defect mitigation**: Precursor purity, ALD purge, post-anneal.
- **Circuit assists**: ECC, adaptive pulses, refresh.
- **Array architecture**: Redundancy/repair, SRAM+FeFET hybrid.

The FeFET's role as SRAM backup (not stand-alone NVM) avoids density stress, improves yield, and enhances reliability for industrial/automotive.

VII. Conclusion

We demonstrated a +1 mask FeFET module on 0.18 μm CMOS, requiring only one ALD tool. Devices achieved endurance > 10^5 cycles and retention > 10 years at 85°C, verified by TZDB, TDDB, endurance and retention analyses. Positioning the FeFET array as a supplementary backup to SRAM—rather than a stand-alone high-density NVM—reduces scaling pressure, improves yield, and enhances reliability for automotive, industrial, and IoT applications. Overall, the method provides a cost-effective path to extend mature-node lifetimes while delivering dependable embedded nonvolatile memory.

Acknowledgment

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Biography

Shinichi Samizo has over 25 years of experience in semiconductor process integration and actuator development. After studying control theory and EM modeling in academia, he joined Seiko Epson in 1997 and worked on 0.35–0.18 μm CMOS logic/memory/HV integration, DRAM, and LCD drivers. Later he contributed to PZT actuator development and the PrecisionCore inkjet head. He is currently an independent researcher, publishing educational materials via the ''Project Design Hub''.