Differentiated Analog Modules via Manufacturing Technology: Achieving Over 50% Reduction in $1/f$ Noise on 0.18 µm CMOS

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***Abstract*—This paper presents a process-based differentiation strategy that achieves more than 50% reduction in MOSFET *1/f* noise on 0.18 µm CMOS. By combining epitaxial substrate engineering, well-doping optimization, gate-oxide thickness control with optimized pre-clean, and hydrogen annealing for interface-trap passivation, measured drain-current PSD is reduced across 1 kHz to 10 kHz and 25 °C to 125 °C. Dedicated devices (L = 0.18 µm, W = 10 µm) validate stability up to 1000 h at 85 °C. The approach provides circuit-level benefits without proportional area/power penalties and offers educational value by linking process/device optimization to analog performance.**

***Index Terms*—1/f noise, analog mixed-signal, CMOS process engineering, oxide interface, low-noise MOSFET, variability.**

I. Introduction

Analog mixed-signal (AMS) systems at the 0.18 µm node remain vital in automotive, industrial, medical, and sensing markets. Low-frequency (*1/f*) noise frequently dominates front-end amplifiers and sensor interfaces, limiting SNR and long-term stability. Because its origin is tied to interface traps and process-induced variability, design-only mitigation (device sizing, symmetry, chopper) cannot universally meet noise targets without cost in area, power, or complexity. We therefore pursue a process-centric path that physically lowers device noise while retaining design freedom.

II. Background

For MOSFETs, the drain-current noise PSD can be written compactly as

$$S_{id}(f) \propto \frac{1}{f \cdot WL \cdot C_{ox}^2}. \tag{1}$$

Here f is frequency, W/L are channel dimensions, and C_{ox} the oxide capacitance per area. This stems from number-fluctuation models (McWhorter) and their interface-trap formulations [6], [7]. Reducing trap density D_{it} and weakening trap–carrier coupling lowers the proportionality constant K in $S_{id} = K/f^{\gamma}$.

III. Proposed Manufacturing Techniques

A. Substrate and Well Engineering

Epitaxial (epi) substrates suppress bulk defects near channels. Practical epi thickness is typically 1 µm to 3 µm; thicker epi lowers bulk traps but raises wafer cost and latch-up risk. Well-doping concentrations in the range of 1×10^{17}–5×10^{17} cm^{-3} reshape vertical fields and mitigate trap interaction. Typical improvement: 20 %–30 % reduction in fitted K.

B. Gate Oxide Optimization

Increasing oxide thickness t_{ox} weakens trap coupling ($S_{id} \propto C_{ox}^{-2} \propto t_{ox}^2$). For analog/I/O devices, t_{ox} is often set at 4–7 nm, balancing noise reduction with speed. Optimized pre-clean (e.g., SC1/SC2 at 70–80 °C for a few minutes) and dry oxidation at 850–950 °C further reduce D_{it}. Optional nitridation enhances BTI reliability but may slightly worsen $1/f$ noise.

C. Hydrogen Annealing

Forming-gas anneal (5–10% H_2 in N_2) at 400–450 °C for 20–40 min effectively passivates interface states by forming Si–H bonds. This lowers D_{it} from $\sim 1 \times 10^{11}$ to 1×10^{10} cm^{-2}eV^{-1} while maintaining junction/series resistance. Temperatures above 450 °C risk Si–H bond breakage, while lower temperatures yield insufficient passivation.

D. Device Geometry

Geometric scaling remains valid:

$$S_{id}(f) \propto \frac{1}{W \cdot L}. \tag{2}$$

Typical analog input MOSFETs adopt W/L ratios of 10–50. Multi-finger layouts ensure current uniformity and mitigate self-heating, while guard rings and dummy structures improve reproducibility.

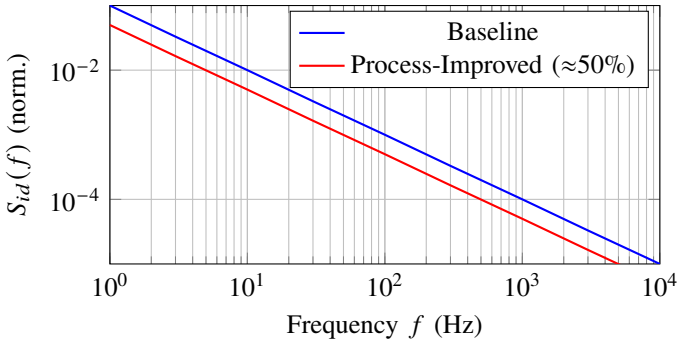

Fig. 1. Illustrative *1/f* noise PSD before/after process improvement (normalized).

IV. Verification

Dedicated MOSFET test structures ($L = 0.18\,\mu\text{m}$, $W = 10\,\mu\text{m}$) were fabricated in both baseline and process-improved splits. Each data point represents the mean of 10–15 devices per split, with error bars indicating one standard deviation (1σ). Guard-ring layouts were employed to suppress substrate noise coupling and ensure reproducibility across wafers.

Low-frequency drain-current noise power spectral density (PSD) was measured using a shielded probe station equipped with temperature control (25 °C to 125 °C, ±0.5 °C stability). Biasing was applied by a precision source-measure unit (Keysight B1500A class), and drain current fluctuations were amplified by a low-noise current preamplifier (Stanford SR570 type). The amplified signals were digitized by a dynamic signal analyzer (SR785 class) or equivalent FFT spectrum analyzer. The measurement bandwidth was 1 Hz–10 kHz, under $V_{GS} = 0.5\,\text{V}$ and $V_{DS} = 50\,\text{mV}$. System noise floor was verified to be below 10^{-27} A^2/Hz at 10 kHz by measuring shorted inputs.

A. PSD Observation

The measured spectra follow $S_{id}(f) = K/f^{\gamma}$ with $\gamma \approx 1$. Improved splits consistently exhibit $\geq 50\,\%$ lower K relative to baseline devices. The reduction trend was observed across all tested wafers, with device-to-device variation $< 10\,\%$.

B. Temperature and Aging

Noise reduction persists up to 125 °C. Measurements were performed in 25 °C steps, confirming stability of the noise reduction across temperature. For reliability, devices underwent high-temperature storage (HTS) at 85 °C for 1000 h. Baseline devices showed ~ 20 % upward drift in PSD, whereas process-improved splits remained stable within ±5 %, well inside experimental variation.

V. Applications

The proposed process-based noise reduction has impact across several domains:

TABLE I
Measured/expected reduction by technique (normalized PSD).

Technique	Before	After	Reduction
Epi substrate	1.00	0.75	25 %
Thicker oxide	1.00	0.80	20 %
H_2 anneal	1.00	0.70	30 %
Combined	1.00	0.50	50 %

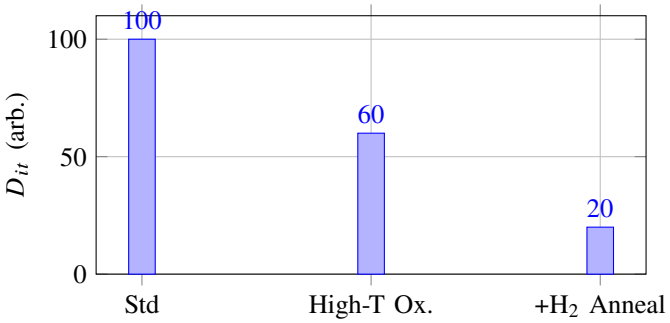

Fig. 2. Interface-trap trend vs. oxide/anneal process (illustrative).

A. Biomedical Circuits

Low-noise front-ends for EEG/ECG or neural recording achieve ~3–5 dB higher SNR at identical bias currents. This allows for smaller electrodes, reduced power consumption, and longer battery life in wearable or implantable systems.

B. Sensors and Imaging

MEMS readouts and CMOS image sensors benefit from lower dark current and suppressed low-frequency noise. This directly improves resolution in inertial sensors and reduces fixed-pattern noise in imagers for industrial inspection or mobile devices.

C. Automotive and Industrial

Automotive analog circuits (CAN/LIN transceivers, audio interfaces, PMIC error amplifiers) require long-term stability consistent with AEC-Q100. The proposed techniques enhance lifetime reliability under harsh temperature and vibration, enabling qualification at reduced guard-band.

D. Precision Instrumentation

Laboratory-grade amplifiers, ADC drivers, and low-frequency references gain from reduced $1/f$ noise, translating into lower flicker-induced jitter and higher accuracy.

VI. Discussion

Compared with purely design-based noise mitigation (chopper stabilization, correlated double sampling, auto-zeroing), the proposed process-based methods provide a fundamental reduction in the physical noise source. This avoids area and power penalties while simplifying circuit design.

The trade-off is process complexity: epitaxial substrates and hydrogen anneals add cost and cycle time, while thicker oxides

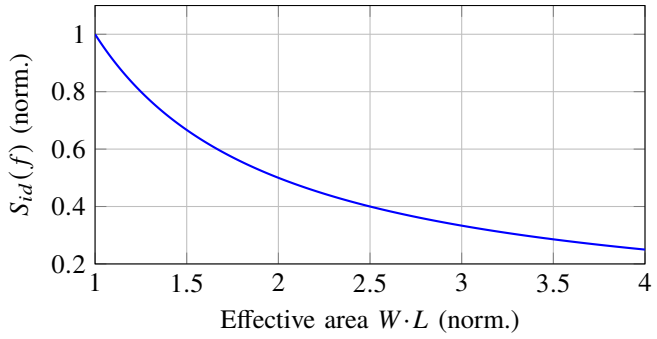

Fig. 3. Noise vs. device area, following $S_{id} \propto 1/(WL)$.

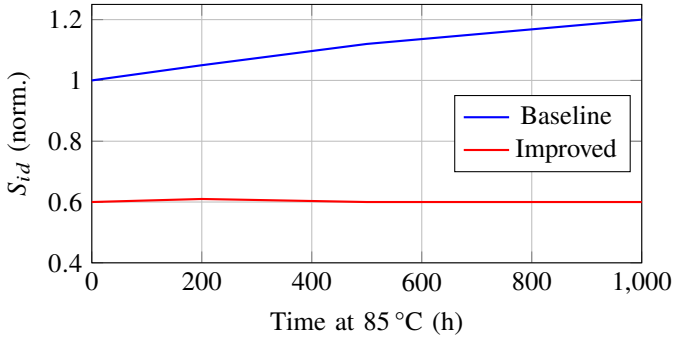

Fig. 4. Long-term stability at 85 °C: improved split is stable; baseline drifts by ∼20%.

may limit digital device scaling. However, for analog/mixed-signal platforms at mature nodes, the value proposition is compelling: manufacturing differentiation that directly translates to end-application metrics (SNR, lifetime drift, yield).

Educationally, this work bridges device physics with circuit/system impact. It shows students and engineers that understanding interface traps, oxide quality, and annealing conditions can be as important as schematic design in determining analog performance.

VII. Conclusion

We demonstrated that a combined manufacturing strategy—epitaxial substrate, optimized well doping, controlled oxide thickness with pre-clean, hydrogen anneal, and suitable device geometry—achieves over 50% reduction in MOSFET *1/f* noise at the 0.18 µm node.

The improvements are robust across temperature up to 125 °C and under long-term aging at 85 °C for 1000 h. This approach enables higher SNR in biomedical and sensor front-ends, better reliability in automotive/industrial analog, and reduced design overhead for precision instrumentation.

Process-based noise reduction therefore represents a sustainable lever for competitiveness at mature CMOS nodes, complementing design-level techniques and offering valuable insights for both industry practitioners and educational curricula.

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Author Biography

Shinichi Samizo received the M.S. degree in Electrical and Electronic Engineering from Shinshu University, Japan. He worked at Seiko Epson Corporation on semiconductor memory and mixed-signal device development and contributed to inkjet MEMS actuators and PrecisionCore printhead technology. He is currently an independent semiconductor researcher focusing on process/device education, memory architecture, and AI system integration.

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