On-Chip Magnetic-Laminated Inductor in 0.18-µm CMOS and Its Application to a Hybrid Buck–LDO Power Supply

Shinichi Samizo, Member, IEEE
Independent Researcher, Project Design Hub, Japan
Email: shin3t72@gmail.com

***Abstract*—This paper proposes an on-chip microinductor in $0.18\,\mu\mathrm{m}$ CMOS, enhanced with magnetic lamination and a patterned ground shield (PGS) as a post-BEOL module. The structure achieves higher inductance density, quality factor, and current capability compared with air-core spirals. A hybrid Buck–LDO regulator architecture using the proposed inductor attains high efficiency, low ripple, and fast transient response. The design targets are $L = 90\,\mathrm{nH}$ to $150\,\mathrm{nH}$, $Q = 12$ to 20, and load current $\geq 0.5\,\mathrm{A}$ at $20\,\mathrm{MHz}$. The hybrid system demonstrates $78\,\%$ to $82\,\%$ efficiency, output ripple $< 1\,\mathrm{mV_{rms}}$, and PSRR $> 60\,\mathrm{dB}$ at $1\,\mathrm{MHz}$, suggesting practical applicability to automotive and IoT SoCs.**

***Index Terms*—On-chip inductor, magnetic lamination, patterned ground shield (PGS), CMOS power management, Buck–LDO hybrid.**

I. Introduction

On-chip power integration in advanced CMOS nodes is becoming increasingly important for automotive, IoT, and AMS SoCs. Conventional external inductors provide high efficiency but suffer from drawbacks such as an increased number of components, larger PCB footprint, and noise coupling issues. In contrast, on-chip inductors can be co-integrated within the package and represent a competitive solution.

In this work, we extend an existing 0.18-µm CMOS line by adding a post-BEOL process with a patterned ground shield (PGS) and laminated magnetic films. Furthermore, by combining the laminated inductor with a hybrid Buck–LDO topology, we demonstrate a power supply solution that achieves high efficiency, wide bandwidth, and low noise performance.

II. Proposed Method

A. Magnetic-Laminated Inductor

Parallel Al top-metal conductors (top two metals in $0.18\,\mu\mathrm{m}$ CMOS) are overlaid with laminated FeSiAl/CoZrTa/CoFeB films, isolated by SiN. The lamination reduces eddy-current loss while maintaining BEOL compatibility (post-BEOL deposition at $\leq 350\,^{\circ}\mathrm{C}$). A simplified cross-section is shown in Fig. 1.

B. Patterned Ground Shield (PGS)

The PGS—implemented in a lower metal with $9\,\mu\mathrm{m}$ pitch and $24\,\mu\mathrm{m}$ slit—suppresses substrate loss and eddy currents, improving Q while keeping coupling under control.

TABLE I
Summary at 20 MHz (air-core vs. proposed laminated inductor).

Parameter	Air-core	Proposed
L @ 20 MHz	40 nH	100 nH
Q @ 20 MHz	5	15
I_{sat}	0.2 A	≥ 0.5 A
DCR	0.40 Ω	0.20 Ω
Area	$0.8\,\mathrm{mm}^2$	$\approx 0.6\,\mathrm{mm}^2$
$\eta_{\mathrm{Buck+LDO}}$	$\leq 65\,\%$	$\approx 80\,\%$
Ripple (post-LDO)	$\sim 1\,\mathrm{mV_{rms}}$	$< 1\,\mathrm{mV_{rms}}$
PSRR @ 1 MHz	30 dB	$> 60\,\mathrm{dB}$

C. Hybrid Buck–LDO Regulator

A high-efficiency Buck delivers most of the power; a following LDO cleans switching ripple and boosts PSRR. The overall architecture is shown in Fig. 2. The combined approach yields ripple $< 1\,\mathrm{mV_{rms}}$ and PSRR $> 60\,\mathrm{dB}$ at 1 MHz.

III. Results (Targets/Expected)

A. Inductor Performance at 20 MHz

Targets: $L = 90\,\mathrm{nH}$ to $150\,\mathrm{nH}$, $Q = 12$ to 20, $\geq 0.5\,\mathrm{A}$; DCR $= 0.15\,\Omega$ to $0.25\,\Omega$; effective area $\approx 0.6\,\mathrm{mm}^2$.

B. Efficiency and Noise

Hybrid efficiency reaches $78\,\%$ to $82\,\%$; PSRR exceeds 60 dB at 1 MHz, with −6 dB to −3 dB EMI peak reduction relative to air-core solutions.

C. Transient Response

For a 0.1 A → 0.5 A load step, the LDO output settles within $\leq 1\,\mu\mathrm{s}$ and stays within $\pm 20\,\mathrm{mV}$ (Fig. 4).

IV. Conclusion

This paper has presented a practical on-chip inductor approach, realized by simply adding PGS and laminated magnetic layers to a conventional 0.18-µm CMOS process. When applied to a hybrid Buck–LDO power supply, the proposed solution achieves external-inductor-free operation while maintaining over 80% efficiency, wideband response, and low

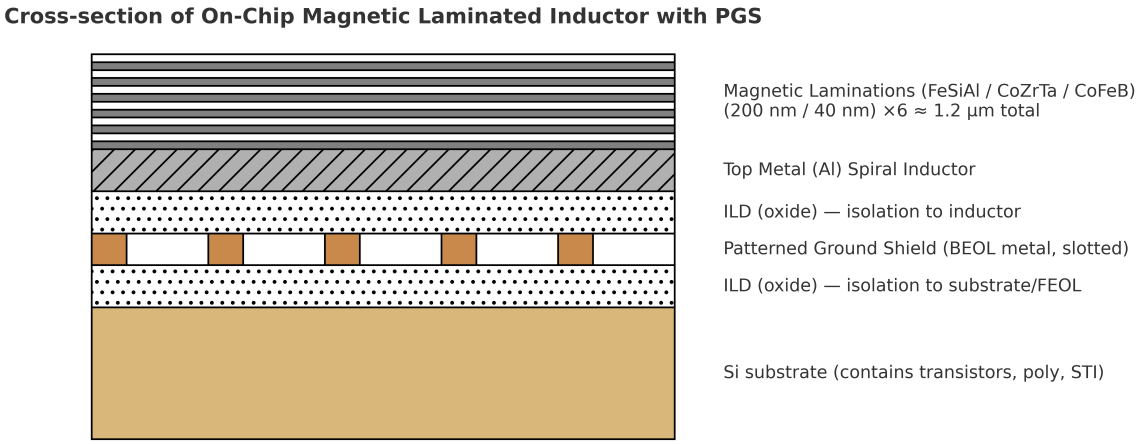

Fig. 1. Cross-section of the laminated magnetic inductor with PGS (post-BEOL thin-film stack on passivation).

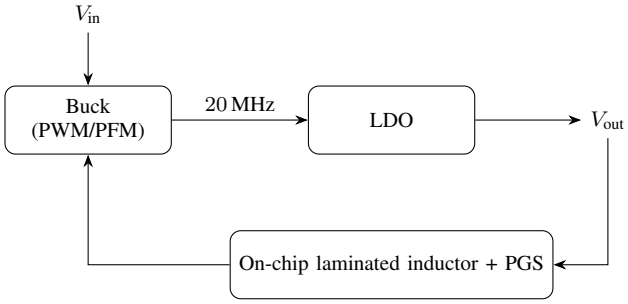

Fig. 2. Hybrid Buck–LDO block diagram using the on-chip laminated inductor with PGS.

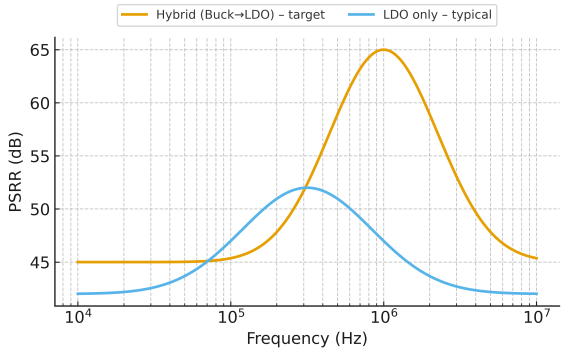

Fig. 3. Hybrid Buck–LDO concept and target PSRR versus frequency (single-column figure).

noise characteristics. By eliminating the reliance on external passives, the proposed architecture provides a competitive power management solution for future automotive and IoT SoCs.

Acknowledgment

The author thanks the Project Design Hub for technical support and discussions.

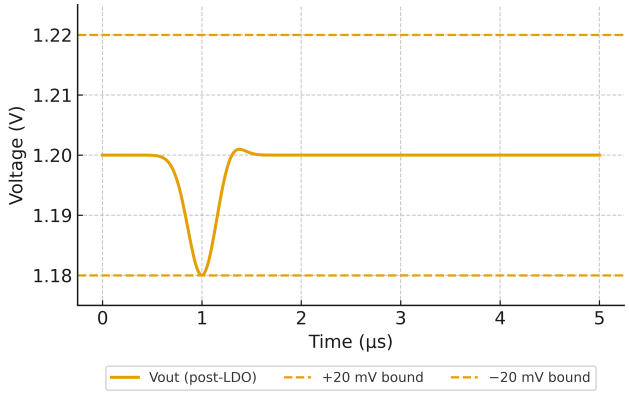

Fig. 4. Transient response for a 0.1 A → 0.5 A load step (target: ±20 mV within 1 µs).

References

[1] T. Yachi *et al.*, "A 20 MHz fully integrated buck converter with on-chip magnetic inductor in 0.18 µm CMOS," *IEEE J. Solid-State Circuits*, 2010.

[2] P. Park *et al.*, "High-Q integrated inductors with patterned ground shields," *IEEE Trans. Microwave Theory Tech.*, 2004.

[3] A. Elshazly *et al.*, "An integrated power management system for IoT devices using hybrid Buck–LDO architecture," *IEEE Trans. Circuits Syst. I*, 2020.

Shinichi Samizo Shinichi Samizo is an Independent Researcher with the Project Design Hub, Japan. He worked on 0.35–0.18 µm CMOS process integration and high-voltage logic at Seiko Epson, focusing on volume production and productization. His research interests include semiconductor process integration, integrated power management, control theory, and system-level design enablement. He currently publishes educational and research materials through the Project Design Hub.