Educational Perspectives on Complementary FETs (CFET): Evolution Beyond GAA and Open Challenges

Shinichi Samizo
Independent Semiconductor Researcher
Project Design Hub, Samizo-AITL
Email: shin3t72@gmail.com *GitHub:* Samizo-AITL

***Abstract*—This tutorial paper provides an educational overview of emerging *Complementary FET (CFET)* technology, which vertically stacks nFET and pFET devices beyond Gate-All-Around (GAA) nanosheets. CFET reframes the CMOS inverter as a *cross-sectional* integration, promising density and delay improvements. We consolidate structure, electrostatic motivations, layout and delay impacts, fabrication challenges, and modeling limitations, and articulate the pedagogical value of CFET as an open, unresolved technology for semiconductor curricula.**

***Index Terms*—CFET, GAA, FinFET, nanosheet FET, short-channel effects, scaling, education, tutorial, vertical stacking, PDK.**

I. Introduction

Scaling has progressed from planar CMOS to FinFET and most recently GAA nanosheet FETs. Beyond the 2 nm node, interconnect delay and cell footprint limit further gains despite excellent electrostatics. CFET stacks nFET and pFET in the vertical dimension so that the cross-section itself constitutes a CMOS inverter, potentially doubling effective standard-cell density while shortening n–p connections. This paper positions CFET as both a roadmap element and an educational vehicle for device–design co-optimization.

II. Device Evolution: From SCE Relief to Cross-Sectional CMOS

Scaling history can be viewed as a sequence of innovations in gate–channel electrostatics. Each generation provided stronger short-channel control, but also introduced new integration bottlenecks that motivated the next architectural shift (see Fig. 1).

A. Planar CMOS: Collapse under SCE

As gate lengths entered the deep sub-100 nm regime, planar MOSFETs suffered severely from short-channel effects (SCE): threshold-voltage roll-off, drain-induced barrier lowering, large off-state leakage, and degraded subthreshold slope. Electrostatic control by a single top gate was insufficient, leading to the collapse of classical planar scaling.

B. FinFET: Three-Sided Gate Recovery

FinFETs restored scalability by wrapping the gate around *three* sides of a vertical fin. The enhanced gate coupling sharpened subthreshold slope, improved variability, and enabled multi-fin drive current scaling per device. However, the tall/narrow fin introduced new trade-offs: sensitivity to line-edge roughness, process variability, and the fact that one side of the channel remained ungated.

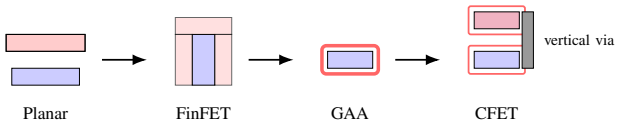

Fig. 1. Device evolution: Planar → FinFET (3-side) → GAA (4-side) → CFET (stacked n/p).

C. GAA Nanosheet: Four-Sided Ideal Control

Gate-All-Around (GAA) nanosheet FETs extended electrostatics to *four* sides by surrounding suspended sheets with the gate. This architecture nearly idealized SCE suppression and variability control, enabling sub-3 nm nodes [1], [2]. Yet, as device electrostatics became nearly perfect, the performance bottleneck shifted toward *wiring*: local interconnect resistance/capacitance (RC) and the lateral footprint of standard cells limited further delay/energy gains.

D. CFET: Cross-Sectional CMOS Integration

Complementary FETs (CFETs) address wiring and density limits by stacking nFET and pFET devices in the *same lateral footprint* and connecting them vertically. Educational takeaways are: (i) effective cell density can nearly double by sharing diffusion/gate footprint across polarities; and (ii) the critical n-to-p connection in inverters and logic networks is shortened, reducing local RC and FO1 delay. In effect, CFET reframes CMOS as a *cross-sectional inverter* rather than a lateral pair [3], [4]. While promising, CFETs also introduce new integration challenges: < 5 nm alignment tolerance, low thermal budget for sequential processing, and inter-tier parasitic coupling.

III. CFET Structural Concepts

Two integration styles are considered, reflecting a likely roadmap progression: first the *Sequential CFET* as the initial candidate, and then the *Forksheet CFET* as a possible successor if inter-tier interference proves problematic (Figs. 3, 4).

TABLE I
TECHNOLOGY NODE EVOLUTION: FROM GAA TO CFET (INDICATIVE VALUES, USEFUL FOR COURSEWORK EXERCISES).

Node (Year)	Device Architecture	VDD (typ.)	Transistor Density (MTr/mm^2)	Notes
7 nm (2018)	FinFET	0.70–0.80 V	90–100	Cell height constraints, multi-patterning EUV
5 nm (2020)	FinFET → pre-GAA	0.65–0.75 V	130–170	First high-volume EUV, RC delay dominant
3 nm (2023)	GAA nanosheet	0.60–0.70 V	200–250	Four-sided electrostatics, variability reduction
2 nm (2025 est.)	GAA production	0.55–0.65 V	300–400	Multi-sheet optimization, DTCO critical
<2 nm (2027–2030)	CFET (stacked n/p)	0.50–0.60 V	500–700	Cross-sectional inverter, vertical RC benefit
1 nm-class (2030+)	Sequential/Forksheet CFET	<0.50 V	>800	3D stacking, thermal-aware BEOL, AI-assisted design

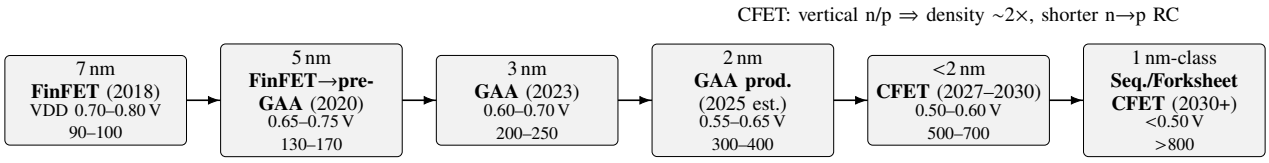

Fig. 2. Compact roadmap timeline aligned with Table I. Values indicative; adapted from IRDS [5] and IMEC [3].

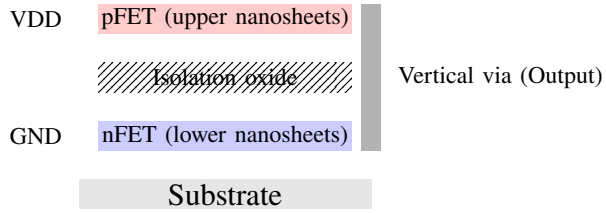

Fig. 3. Sequential CFET cross-section: stacked nFET/pFET with vertical output via. Current research focuses on managing parasitic coupling and thermal interference in this architecture.

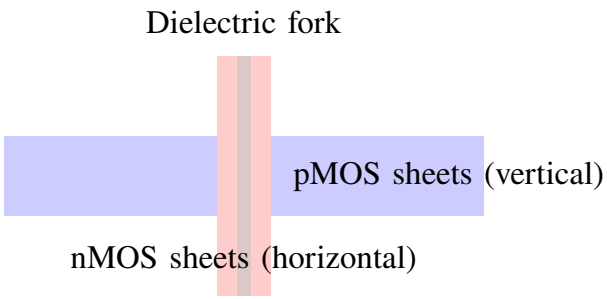

Fig. 4. Forksheet CFET top view: orthogonal n/p nanosheets with a dielectric fork. This style is envisioned as a follow-up option if Sequential CFET coupling proves too limiting.

(i) Sequential CFET: The first integration style expected in practice is the Sequential CFET. Here, the nFET tier is fabricated first, followed by the pFET tier stacked above it under a constrained thermal budget. Selective epitaxy/etch and dielectric isolation are crucial, as is vertical contact to the inverter output. Because n- and p-devices are stacked in close proximity, however, concerns arise regarding electrostatic coupling, vertical via parasitics, and thermal interference between tiers.

(ii) Forksheet CFET: If interference in Sequential CFETs becomes too severe, a next-step option is the Forksheet CFET. In this style, n- and p-channels are placed orthogonally and separated by a dielectric "fork" spacer. This geometry helps mitigate inter-tier parasitics, preserves electrostatic control, and eases routing congestion.

IV. ELECTRICAL AND LAYOUT IMPACTS

CFET integration affects not only cell density but also delay, variability, and power distribution in ways that extend beyond GAA devices. Key educational points include:

- **Area efficiency:** By vertically stacking nFET and pFET within the same lateral footprint, inverter density can approach nearly 2×. This benefit extends to complex logic cells (e.g., NAND/NOR) by co-locating pull-up and pull-down networks in the same footprint. Students should recognize how this structural gain cascades into standard-cell library design and physical design rules such as *cell height* and *routing pitch*.
- **Delay/energy:** The vertical n-to-p via drastically shortens the inverter's RC path compared to lateral wiring in GAA. Even if individual *I–V* curves remain similar to GAA, FO1 delay and stage energy are improved due to reduced interconnect length. This highlights the shift of scaling benefit from device *I–V* to *wiring geometry*.
- **Electrostatics:** Each tier can retain GAA-level control, but inter-tier dielectric/field coupling introduces new parasitics (capacitance, via resistance). This provides an excellent tutorial case where device electrostatics interact with circuit parasitics, requiring students to think about multi-physics co-optimization.
- **Variability/noise:** Vertical stacking introduces thermal coupling between tiers, causing asymmetric heating of n/p devices. Furthermore, VDD and GND partitioning across layers generates uneven IR drop and noise susceptibility. These effects demand new placement and routing strategies, illustrating how device innovations ripple up into CAD tool requirements.

From a teaching perspective, this section demonstrates how *device-level innovations directly translate into EDA challenges*, making CFET a natural case study in DTCO curricula.

V. Manufacturing Challenges

Realizing CFETs requires overcoming fabrication hurdles that exceed previous scaling transitions. Independent n/p work-functions and junctions across stacked tiers demand highly selective epitaxy and etching, often under low thermal budgets ($< 500^{\circ}$C) to avoid damaging the completed tier. Vertical via alignment must achieve sub-5 nm overlay, pushing EUV lithography beyond current production standards. Dielectric isolation must simultaneously suppress dopant diffusion and preserve mechanical integrity across multiple stacked layers.

Recent demonstrations by IMEC indicate that sequential CFETs are feasible at the research level [3]. However, industrial-scale yield, variability control, and long-term reliability remain unresolved. In particular, *independent threshold-voltage tuning of nFET/pFET tiers* is critical for SRAM stability and large-scale logic integration. This makes CFET a rich topic for classroom debate on manufacturability versus theoretical scaling.

VI. Modeling and EDA Limitations

Existing compact models such as BSIM-CMG can capture GAA device behavior, but extensions to CFET remain absent. Key missing aspects include:

1) Inter-tier electrostatics and capacitive coupling,
2) Vertical thermal interactions between stacked devices,
3) Parasitic RC from vertical vias and tier-to-tier contacts.

Prototype Verilog-A models have been proposed but lack consensus, calibration, and reproducibility. Furthermore, no open-source CFET-ready PDKs or standard-cell libraries are available, preventing standardized design flows. From an educational perspective, this modeling gap provides fertile ground for coursework: students can extend compact models, explore sensitivity analysis, and appreciate the impact of missing parasitics on design predictions. This gap is also echoed in the IRDS roadmap [5].

VII. Toward a CFET-Aware Compact Model

While BSIM-CMG has become the de facto standard for FinFET and GAA nanosheet devices, an extension toward CFET requires explicit modeling of *cross-tier interactions*. Key ingredients for a "BSIM-CFET" framework would include:

- **Inter-tier parasitic coupling:** Coupling capacitance (C_{np}) and resistance (R_{np}) between stacked nFET and pFET tiers, influencing inverter delay, noise margin, and dynamic power.
- **Thermal coupling:** Vertical self-heating and cross-heating effects captured through thermal resistance (R_{th}) and capacitance (C_{th}), affecting threshold voltage shift and drive-current degradation.
- **Mechanical stress:** Strain induced by sequential epitaxy and dielectric stacks alters carrier mobility (μ_n, μ_p). Compact models can adopt stress-aware correction terms, e.g., $\mu = \mu_0(1 + \alpha \cdot \sigma)$.
- **Cross-sectional inverter abstraction:** Treating the n/p stack as a single compact "CFET inverter element," where device-to-device interactions are parameterized rather than purely lateral.

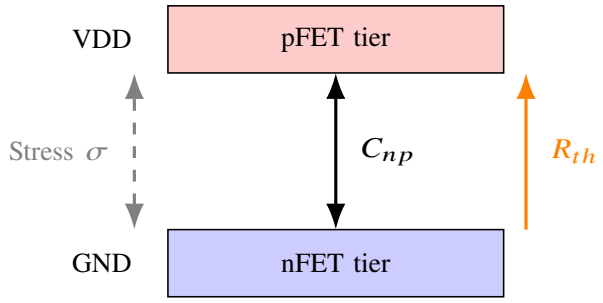

Fig. 5. Conceptual BSIM-CFET compact model extension: stacked nFET/pFET with inter-tier coupling capacitance (C_{np}), thermal resistance (R_{th}), and stress-aware mobility correction (σ).

From an educational standpoint, introducing these extensions provides students a fertile playground for *multi-physics-aware compact modeling*. Exercises can involve sensitivity sweeps of C_{np}, R_{th}, or stress parameters, bridging the gap between device physics and DTCO-level impacts.

VIII. Educational Value

From a pedagogical perspective, CFET is more than a new device—it is a framework for integrating physics, process, layout, and CAD. Graduate courses can incorporate:

- CFET Verilog-A models as design projects,
- Sensitivity studies to inter-tier parasitics,
- Placement/routing co-optimization exercises,
- Roadmap-based discussions linking IRDS forecasts with design-technology co-optimization (DTCO).

Instructors can also differentiate usage scenarios: undergraduate courses may use CFET as a case study of scaling limits and integration hurdles, while graduate curricula can involve hands-on modeling, layout co-optimization, and system-level DTCO studies. This dual-level approach illustrates how CFET can serve as both an introduction to scaling challenges and an advanced platform for design research.

IX. Conclusion and Outlook

CFET reframes CMOS as a stacked, cross-sectional inverter that simultaneously improves density and wiring delay. Looking forward, several research vectors emerge [4], [5]:

- Forksheet CFET layouts to mitigate inter-tier interference,
- 3D sequential stacks under constrained thermal budgets,
- Thermal-aware power partitioning across vertical tiers,
- Co-optimized BEOL integration to reduce parasitic loading,
- AI-driven exploration of design space for DTCO.

Embedding CFET into semiconductor curricula not only prepares engineers for the 2030s, but also fosters critical thinking about unresolved challenges at the scaling frontier—where physics, fabrication, and system design converge.

Acknowledgment

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References

[1] K. Cao, C. Hu *et al.*, "Bsim-cmg: Standard compact model for multi-gate transistors—extensions for gaa nanosheet fets," in *Proc. International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, 2017, pp. 31–34.

[2] N. Loubet, V. Moroz, T. Hook *et al.*, "Stacked nanosheet gate-all-around cmos transistors for sub-3nm nodes," in *Proc. IEEE Symposium on VLSI Technology*, 2019, pp. T194–T195.

[3] N. Yakimets, N. Loubet, Z. Tokei, G. Eneman, A. Veloso, A. Mercha *et al.*, "Integration challenges for cfet (complementary fet) for sub-3nm nodes," in *Proc. IEEE International Electron Devices Meeting (IEDM)*, 2020, pp. 11.3.1–11.3.4.

[4] J.-P. Colinge and A. Veloso, "Complementary fet (cfet) devices: Opportunities and challenges," *Solid-State Electronics*, vol. 186, p. 108100, 2021.

[5] IRDS, "International roadmap for devices and systems 2023 edition," https://irds.ieee.org/roadmap-2023, 2023, accessed: 2025-09-07.

Author Biography

Shinichi Samizo received the M.S. degree in Electrical and Electronic Engineering from Shinshu University, Japan. He worked at Seiko Epson Corporation as an engineer in semiconductor memory and mixed-signal device development, and also contributed to inkjet MEMS actuators and PrecisionCore printhead technology. He is currently an independent semiconductor researcher focusing on process/device education, memory architecture, and AI system integration.

Contact: shin3t72@gmail.com, Samizo-AITL