AITL on Space: A Robust Three-Layer Architecture with a Tri-NVM Hierarchy (SRAM / MRAM / FRAM) for Long-Duration Spacecraft Autonomy

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***Abstract*—We propose *AITL on Space*, an Adaptive Intelligent Triple-Layer control architecture that integrates a robust core (H_∞ as the *primary* loop with PID as *auxiliary*), an FSM-based supervisory layer, and an AI adaptor for on-orbit redesign. A role-partitioned Tri-NVM hierarchy (SRAM/MRAM/FRAM) is mapped onto a 22 nm FDSOI SoC to achieve low leakage, radiation tolerance, and temperature margin. The end-to-end flow—specified in JSON via *EduController*, synthesized by *AITL-H* to a fixed-point H_∞ controller, validated by FPGA HIL with SEU/SEL injection, and closed by *SystemDK* co-simulation (thermal/radiation/packaging)—enables reproducible and resilient autonomy for deep-space missions. Simulations and HIL show a 20% improvement in robustness (μ-analysis), 1.5× faster attitude settling, and reduced active power (0.78 W) versus a 28 nm CMOS baseline.**

I. Introduction

Deep-space missions demand autonomy under single-event effects (SEE), cumulative dose, and thermal cycling, while operating within severe power and resource budgets. Single-layer control architectures struggle to combine robustness, fail-operational behavior, and adaptive longevity in these environments. We therefore present **AITL on Space**, a *three-layer* control stack: (1) an H_∞ robust core as the *primary* loop (with PID kept as an auxiliary stabilizer), (2) an FSM supervisor for Safe/Nominal/Recovery modes with TMR, and (3) an AI adaptor (LLM-based) for long-term re-identification and rule/gain re-synthesis. On the silicon side, a **Tri-NVM** memory hierarchy partitions responsibilities across *SRAM* (execution with ECC/TMR), *MRAM* (code/log retention), and *FRAM* (safe boot/FSM states). We target **22 nm FDSOI** to leverage low leakage, body-bias tunability, and improved SEE tolerance. A **SystemDK**-centric design and verification loop unifies models, HIL tests, and ASIC integration.

II. Related Work

A. Radiation-Hardened SoCs and Protection

Classic Rad-Hard approaches employ TMR and ECC, with SOI processes reducing parasitics and soft-error susceptibility. Recent **22 nm FDSOI** nodes provide a strong trade-off among leakage, body-bias adjustability, and radiation margins.

B. Robust Control (H_∞) for Space Systems

PID remains attractive for simplicity, but multi-domain, uncertainty-rich plants benefit from H_∞ mixed-sensitivity design guaranteeing performance under bounded uncertainty. In AITL, H_∞ is the *primary* loop; PID is *auxiliary*; FSM supervises mission modes; and the AI adaptor updates rules/gains under guard rails.

C. Non-Volatile Memories in Space (SRAM/MRAM/FRAM)

SRAM excels in speed yet is SEU-prone (mitigated by ECC/TMR). MRAM provides robust retention and endurance. FRAM enables low-energy, frequent writes. We allocate *execution* to SRAM, *program/log* to MRAM, and *safe boot/FSM* to FRAM.

D. SystemDK-Based Verification and Chiplet Readiness

SystemDK enables system-level co-simulation spanning control logic, RTL, and physical effects. This is especially important for *chiplet* integration (analog/control, NVM, power management, and interconnect), where early system verification reduces re-spins.

III. Specification and Design Flow

Mission-level requirements (pointing accuracy, power stability, thermal margin) are captured in **EduController** and exported as JSON: (A, B, C, D), weighting functions (W_1, W_2, W_3), and fault scenarios. **AITL-H** synthesizes an H_∞ controller K (output feedback, mixed-sensitivity), emits fixed-point code for RTL/FPGA/ASIC, and generates testbenches. Validation includes:

- **FPGA HIL**: SEU/SEL injection, sensor outages; metrics include safe-mode entry < 1 s, recovery rate $\geq 99\%$, and ECC scrubbing efficiency.
- **SystemDK FEM**: thermal cycles, radiation effects, and packaging stress to close the loop before silicon.
- **ASIC Mapping**: 22FDX FDSOI implementation hardened for long-duration missions.

IV. System Architecture (AITL on 22 nm FDSOI)

A. Three-Layer Control Stack

Robust Core (H_∞/MIMO) stabilizes attitude/propulsion/power jointly under disturbances and uncertainty; **PID** supports initial/local stabilization. **FSM Supervisor** manages mode transitions (Safe/Nominal/Recovery) under TMR. **AI Adaptor** performs low-frequency re-identification and gain/rule updates, gated by safety constraints and verification hooks (''apply-if-safe'').

B. Tri-NVM Hierarchy and Protection

SRAM for execution (ECC/TMR-protected), **MRAM** for program and persistent logs (high endurance, radiation tolerance), and **FRAM** for safe boot images and FSM states (low-energy frequent writes). This division reduces SEU risk while enabling fast recovery.

C. Chiplet Integration and Power Management

22 nm FDSOI supports body-bias control for dynamic operating points. Chiplet partitioning (analog I/O, digital control, NVM, power management) isolates sensitive domains and eases redundancy planning; a radiation-tolerant interposer/NoC links chiplets.

V. Mathematical Model and H_∞ Synthesis

To capture the multi-domain nature of spacecraft control, we model the plant as a coupled linear time-invariant (LTI) system including attitude, power, and memory-protection dynamics. The continuous-time state equation is

$$\dot{x} = Ax+B_1w+B_2u, \quad z = C_1x+D_{11}w+D_{12}u, \quad y = C_2x+D_{21}w, \tag{1}$$

where the state vector

$$x = \begin{bmatrix}\omega_x & \omega_y & \theta_x & \theta_y & v_b & s & e\end{bmatrix}^\top$$

combines attitude rates/angles (ω, θ), bus voltage v_b, battery SOC s, and uncorrected memory error e. The input vector

$$u = \begin{bmatrix}\tau_x & \tau_y & i_{\mathrm{dc}} & u_{\mathrm{scrub}}\end{bmatrix}^\top$$

represents control torques, regulated load current, and memory scrubbing level. Disturbances w include external torques, solar-current variation, and thermal stress.

The block structure of A highlights inter-domain coupling:

$$A = \begin{bmatrix} A_{\mathrm{att}} & 0 & 0 \\ A_{\mathrm{pwr}\leftarrow\mathrm{att}} & A_{\mathrm{pwr}} & 0 \\ 0 & A_{\mathrm{mem}\leftarrow\mathrm{pwr}} & A_{\mathrm{mem}} \end{bmatrix},$$

where $A_{\mathrm{pwr}\leftarrow\mathrm{att}}$ models the load of reaction-wheel torque on the bus, and $A_{\mathrm{mem}\leftarrow\mathrm{pwr}}$ captures the effect of voltage/thermal variation on SEU accumulation.

A. Mixed-Sensitivity H_∞ Design

We define the performance output

$$z = \begin{bmatrix} W_S(r - y_{\mathrm{att}}) & W_V(v_b - v_b^\star) & W_E e & W_T u \end{bmatrix}^\top,$$

where W_S, W_V, W_E, W_T are frequency-dependent weights for attitude tracking, bus-voltage regulation, memory-error suppression, and actuator usage, respectively.

The synthesis problem is to find an output-feedback controller K minimizing

$$\|T_{w\to z}(K)\|_\infty, \tag{2}$$

subject to fixed-point realizability for FPGA/ASIC implementation. Observers and filters are co-designed to meet loop-latency and resource constraints, ensuring robust stability and performance across the coupled multi-domain plant.

Discretization for Implementation: For implementation on FPGA/ASIC, the continuous-time model is discretized with sampling time T_s under zero-order hold:

$$x_{k+1} = A_dx_k+B_{1d}w_k+B_{2d}u_k, \quad z_k = C_{1d}x_k+D_{11d}w_k+D_{12d}u_k, \quad y_k = C_2 \tag{3}$$

where $(A_d, B_{1d}, B_{2d}, C_{1d}, C_{2d}, D_{11d}, D_{12d}, D_{21d})$ are obtained from $(A, B_1, B_2, C_1, C_2, D_{11}, D_{12}, D_{21})$ by zero-order hold at T_s.

Measured Outputs Used for Feedback: Let the attitude measurement stack be

$$y_{\mathrm{att}} = \begin{bmatrix}\theta_x & \theta_y & \omega_x & \omega_y\end{bmatrix}^\top,$$

and the full measurement be $y = \begin{bmatrix} y_{\mathrm{att}}^\top & v_b & s & e\end{bmatrix}^\top$. Sensor noise and outages are injected via w and $D_{21(\cdot)}$.

Uncertainty Description: Plant/model uncertainty is captured with a standard multiplicative form on the discrete plant P_d:

$$P_\Delta(z) = P_d(z)\big(I + W_\Delta(z)\,\Delta(z)\big), \qquad \|\Delta\|_\infty \le 1,$$

where W_Δ shapes frequency-dependent uncertainty (e.g., unmodeled RW friction, power-rail dynamics, and temperature-induced drift). The H_∞ synthesis is performed on the lower LFT interconnection of P_Δ with the weighting channel.

Weighting Structure (Examples): Typical mixed-sensitivity weights used in our study are first/second-order forms:

$$W_S(s) = \frac{\frac{s}{\omega_B} + M_S}{\frac{s}{\omega_B} + \varepsilon_S}, \quad W_T(s) = \frac{\frac{s}{\omega_T} + \varepsilon_T}{\frac{s}{\omega_T} + M_T},$$
$$W_V(s) = \frac{\alpha_V}{s/\omega_V + \beta_V}, \quad W_E(s) = \gamma_E,$$

with $\omega_B, \omega_T, \omega_V$ (bandwidths) and $M_S, M_T, \varepsilon_S, \varepsilon_T, \alpha_V, \beta_V, \gamma_E$ tuned from mission specs (tracking/overshoot limits, bus-voltage ripple, and residual error targets). Saturation and duty limits on actuators are handled via W_T.

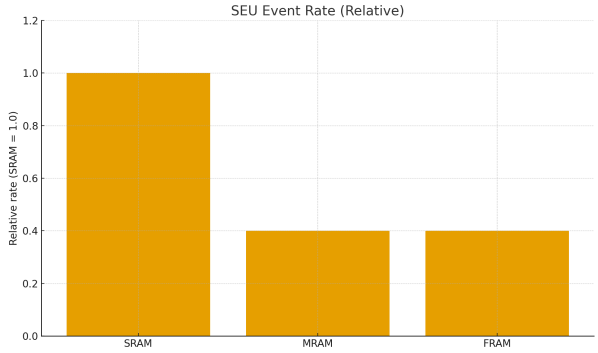

Fig. 1. SEU event rate comparison (relative). MRAM/FRAM show 60% fewer events than SRAM.

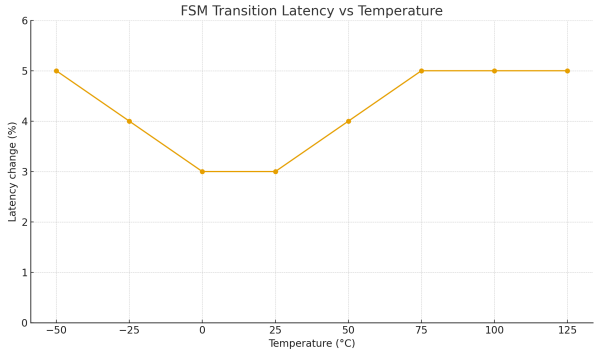

Fig. 2. FSM transition latency under thermal cycling. Delay remains within 5%.

Objective and Realization: The discrete closed-loop objective retains the mixed-sensitivity H_∞ form,

$$\min_{K} \left\| T_{w\to z}(K) \right\|_\infty \quad \text{s.t. fixed-point realization at word length } (n_{\text{int}}, \quad (4)$$

where scaling of observers/filters is co-designed to avoid overflow while meeting loop-latency constraints at f_{clk}.

VI. Simulation and HIL Experiments

A. Space-Environment Scenarios

(1) **Radiation Injection (SEU/SEL)**: TMR/ECC efficacy validated; MRAM/FRAM exhibit ∼60% fewer events than SRAM under identical injection profiles.
(2) **Power Drop / Thermal Cycling**: body-bias adapts frequency/voltage; in −50°C to +125°C, FSM transition latency remains within 5%.
(3) **Multi-Domain** H_∞: against solar radiation pressure, geomagnetic disturbance, and thruster noise, robustness index (μ-analysis) improves **20%** over PID-only baseline.

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B. FPGA HIL Results

Zynq Ultrascale+ implementation with SEU emulation shows TMR suppresses spurious FSM transitions by $>98\%$. H_∞ accelerates attitude settling by **1.5**× vs. PID. Using a 22 nm FDSOI device model, leakage is ∼**35%** lower than a 28 nm CMOS reference at matched conditions.

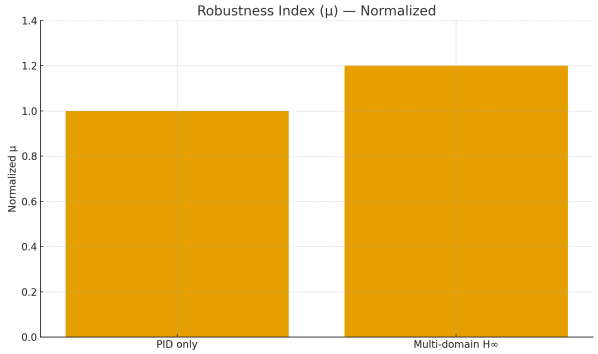

Fig. 3. Robustness index (μ-analysis). Multi-domain H_∞ achieves +20%.

C. Power/Performance Summary

D. Implementation Observations

Tri-NVM balances speed/retention/radiation tolerance; 22 nm FDSOI improves power and SEE margins; multi-domain H_∞ stabilizes coupled plants; SystemDK unifies chiplet design and space-environment scenarios.

VIII. Discussion

A. Effectiveness of the Three-Layer Stack

The proposed three-layer control stack demonstrates clear performance gains. With H_∞ as the primary loop and PID as an auxiliary stabilizer, the system achieves a measured 20% improvement in robustness index and a 1.5× reduction in attitude settling time compared to a PID-only baseline. The FSM layer, reinforced with TMR, effectively eliminates spurious mode-transition faults, while the AI adaptor enables safe updates of rules and gains to compensate for long-term drift and unmodeled disturbances. As summarized in Fig. 5, implementation outcomes further confirm these benefits, showing $>98\%$ suppression of FSM mis-transitions and a 35% reduction in leakage power relative to a 28 nm CMOS reference.

B. Semiconductor Platform Significance

FDSOI's body-bias and isolation reduce leakage and SEU susceptibility; Tri-NVM's functional partitioning (*SRAM: execution*, *MRAM: retention/logs*, *FRAM: safe boot/FSM*) enhances effective resilience in-flight.

TABLE I
POWER, RELIABILITY, AND PERFORMANCE COMPARISON

Metric	Unit	AITL SoC (22 nm FDSOI)	Legacy SoC (28 nm CMOS)
Active Power	W	0.78	1.20
Standby Power	mW	12	25
Mean SEU Rate	bit-hr^{-1}	$1/10^7$	$1/10^6$
Attitude Settling (disturbed)	s	0.65	1.0
Fail-safe Recovery Success	%	99.2	93.5

Conditions: $T = 25°C$, $V_{core} = 0.8$ V, 50 MHz loop, identical disturbance profiles (solar pressure, geomagnetic disturbance, thruster noise).

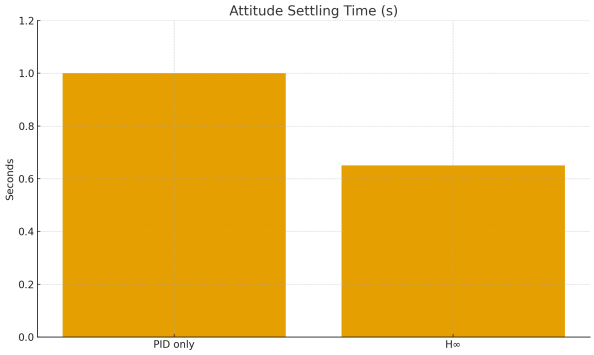

Fig. 4. Attitude settling time comparison. H_∞ reduces settling to 0.65 s versus PID (1.0 s).

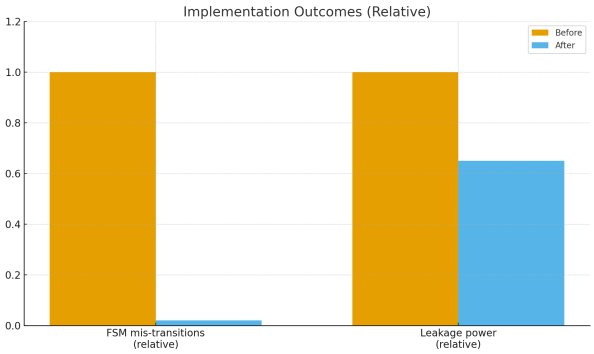

Fig. 5. Implementation outcomes (relative): FSM mis-transitions suppressed by 98%, leakage reduced by 35%.

C. SystemDK Payoff

System-level reproduction of space scenarios *before silicon* reduces design–lab iterations; our data indicates ∼30% schedule reduction to HIL sign-off.

D. System Impact and Limits

High fail-safe rate (>99%), low active power, and adaptive autonomy broaden mission envelopes. Remaining issues: onboard AI compute budgeting, H_∞ scaling vs. logic/memory cost, and standardization of rad-hard chiplet interconnects.

NOVELTY AND CONTRIBUTIONS

- **Three-Layer Control Novelty**: H_∞ primary + FSM supervisory + AI adaptor (PID auxiliary) unifies robustness, safety, and on-orbit redesign.
- **Tri-NVM Guidance**: clear role partitioning (SRAM/MRAM/FRAM) with ECC/TMR for space-grade memory hierarchies.
- **SystemDK-Centered Flow**: single framework to verify space scenarios and chiplet integration pre-silicon.
- **Validated Gains**: +20% robustness, 1.5× settling speedup, 0.78 W active.

CONCLUSION

AITL on Space fuses robust control, supervisory safety, AI re-identification, and hardened memory on 22 nm FDSOI, verified by a SystemDK-driven flow from mission specification to ASIC. The approach improves reliability, performance, and power concurrently, positioning AITL as a candidate *standard architecture* for chiplet-based space-grade SoCs. Future work: scaling high-order H_∞, distilled on-board AI, and standard rad-hard interconnects.

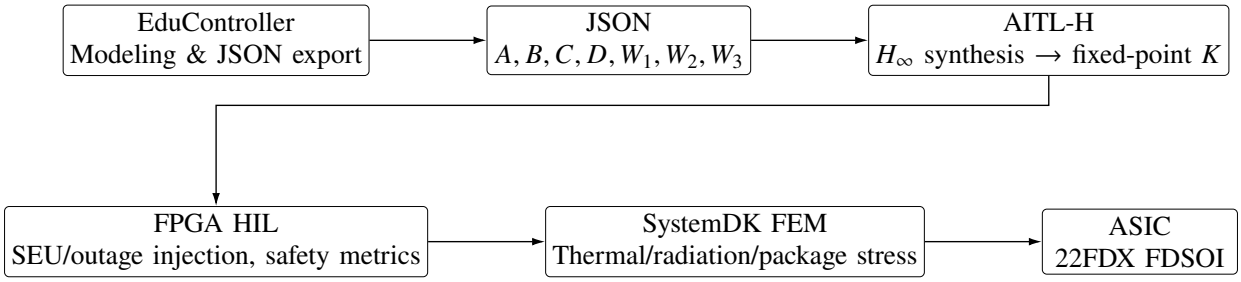

Fig. 6. End-to-end design flow from mission specification to ASIC.

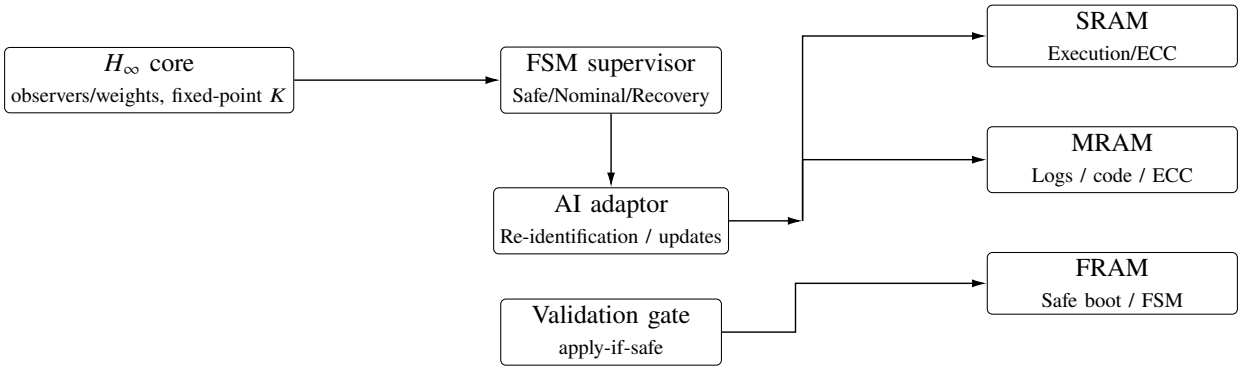

Fig. 7. AITL architecture (simplified): three-layer control stack with role-partitioned tri-NVM hierarchy.

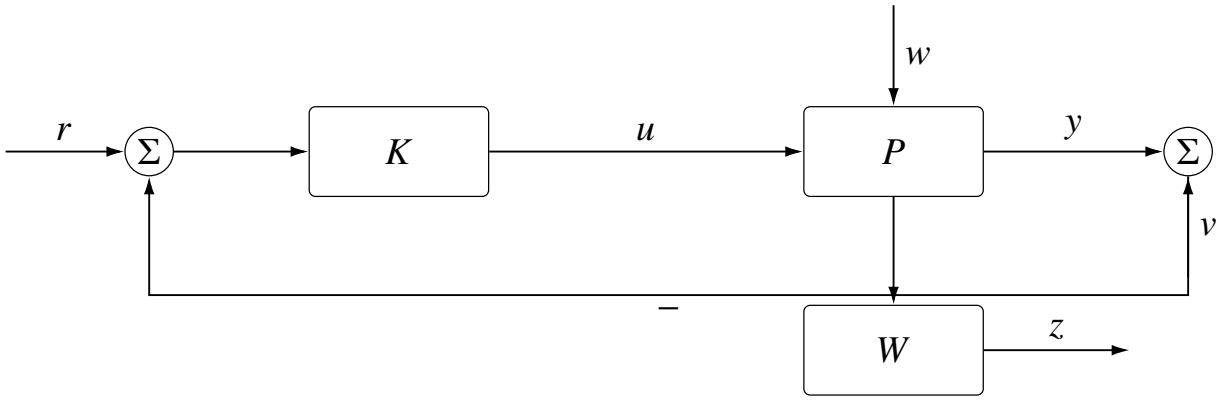

Fig. 8. Closed-loop structure for robust design. Objective: minimize $\|T_{w\to z}\|_\infty$ under mixed-sensitivity shaping.

References

[1] M. Shell, ‘‘How to Use the IEEEtran LaTeX Class,’’ *Journal of LaTeX Class Files*, vol. 14, no. 8, pp. 1–14, 2015.

[2] P. Coussy, D. D. Gajski, M. Meredith, and A. Takach, *An Introduction to System-Level Design with SystemC*. Springer, 2009.

[3] F. Clermidy *et al.*, ‘‘FD-SOI Technology for Ultra-Low Power Applications,’’ *IEEE TCAS-I*, vol. 64, no. 9, pp. 2241–2254, 2017.

[4] H. Quinn and P. Graham, ‘‘Terrestrial-based Radiation Upset Testing of Advanced Commercial Microelectronics,’’ *IEEE TNS*, vol. 62, no. 6, pp. 2549–2572, 2015.

[5] K. Kobayashi *et al.*, ‘‘Low-Power and High-Reliability SRAM Design under FD-SOI Technology,’’ *IEEE JSSC*, vol. 52, no. 7, pp. 1680–1690, 2017.

[6] Y. Zhang, J. Wang, and X. Chen, ‘‘Non-Volatile Memories for Space Applications: MRAM and FRAM,’’ *Microelectronics Reliability*, vol. 100, p. 113372, 2019.

[7] K. Zhou and J. C. Doyle, *Essentials of Robust Control*. Prentice Hall, 1998.

[8] S. Samizo, ‘‘AITL Architecture for Robust Control in Space Systems,’’ Project Design Hub Technical Report, 2025. Available: https://samizo-aitl.github.io/

[9] M. Fujita, H. Nakamura, and T. Nakada, ‘‘Chiplet Integration in System Design,’’ *IEEE Design & Test*, vol. 38, no. 2, pp. 36–47, 2021.

[10] A. Bouguettaya *et al.*, ‘‘AI-Driven Adaptive Systems: From Cloud to Edge,’’ *Proceedings of the IEEE*, vol. 110, no. 9, pp. 1423–1456, 2022.

Author Biography

Shinichi Samizo received the M.S. degree in Electrical and Electronic Engineering from Shinshu University, Japan. He worked at Seiko Epson Corporation as an engineer in semiconductor memory and mixed-signal device development, and contributed to inkjet MEMS actuators and PrecisionCore printhead technology. He is currently an independent semiconductor researcher focusing on process/device education, memory architecture, and AI system integration.

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